Compal confidential

Schematics Document

Mobile P4 uFCBGA/uFCPGA with INTEL MONTARA-GML/ICH4-M core logic

2002-02-10

REV:1.0

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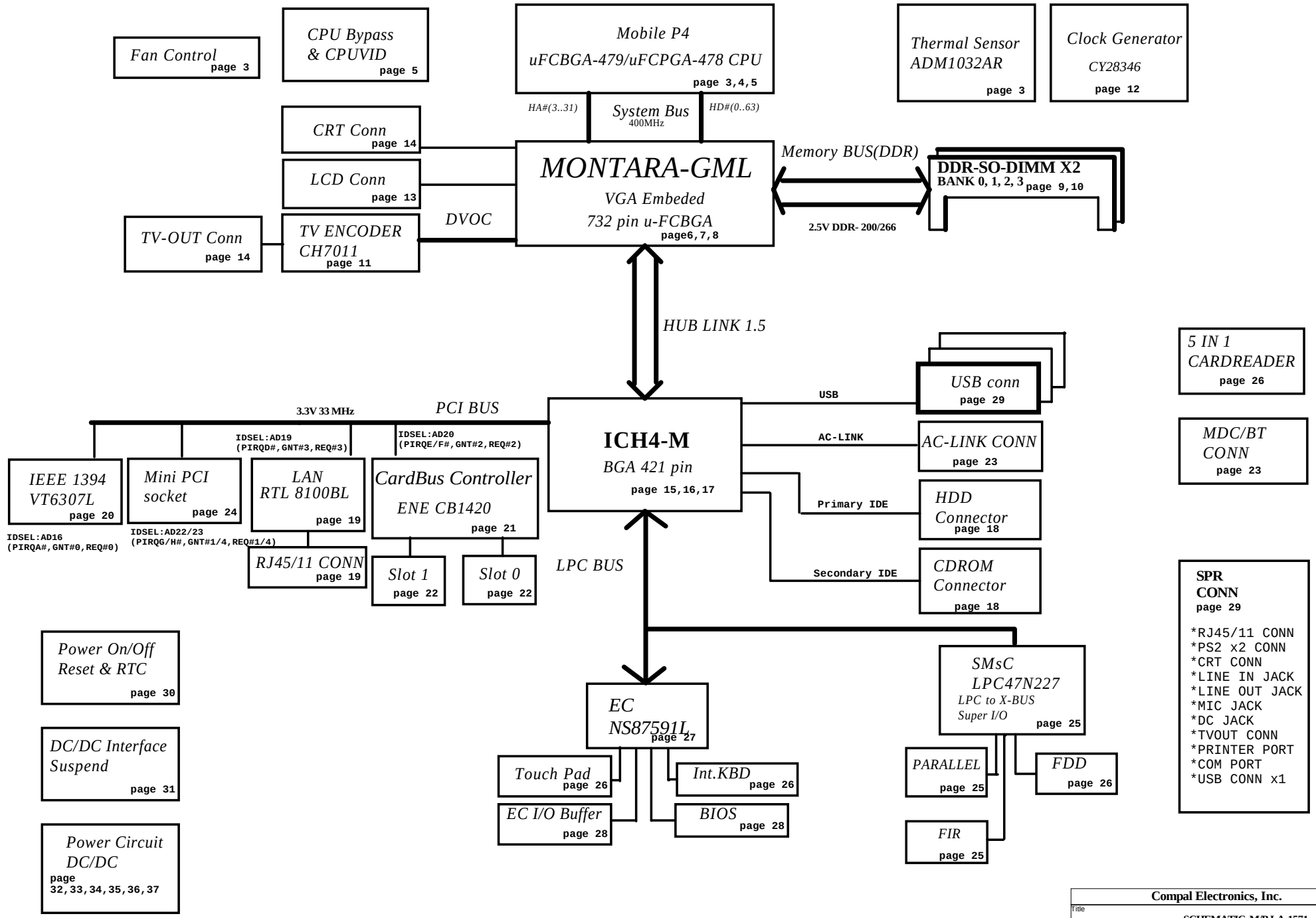
File Name : LA-1571



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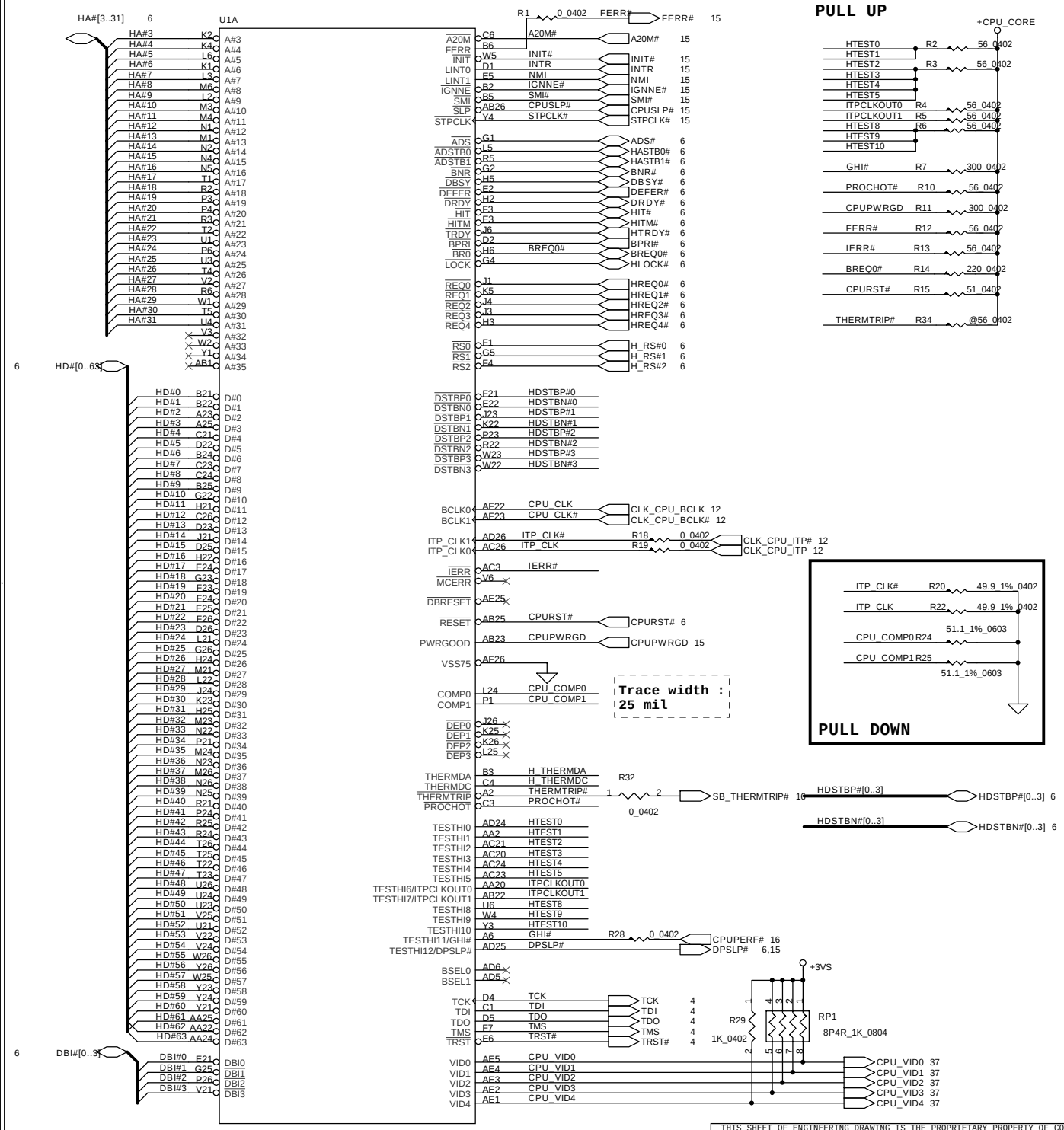
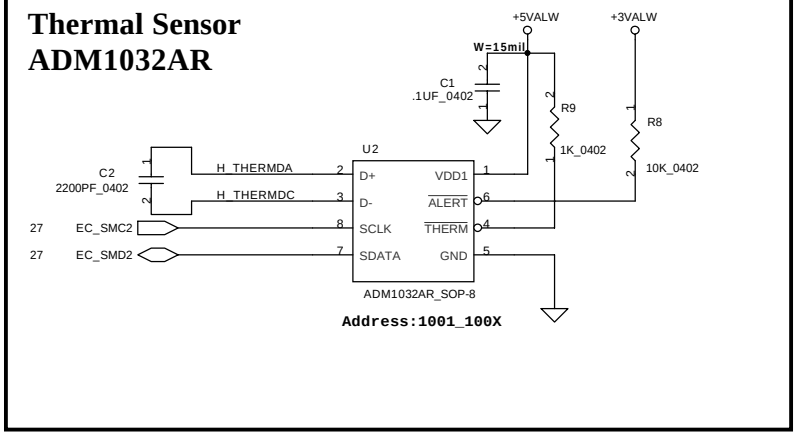
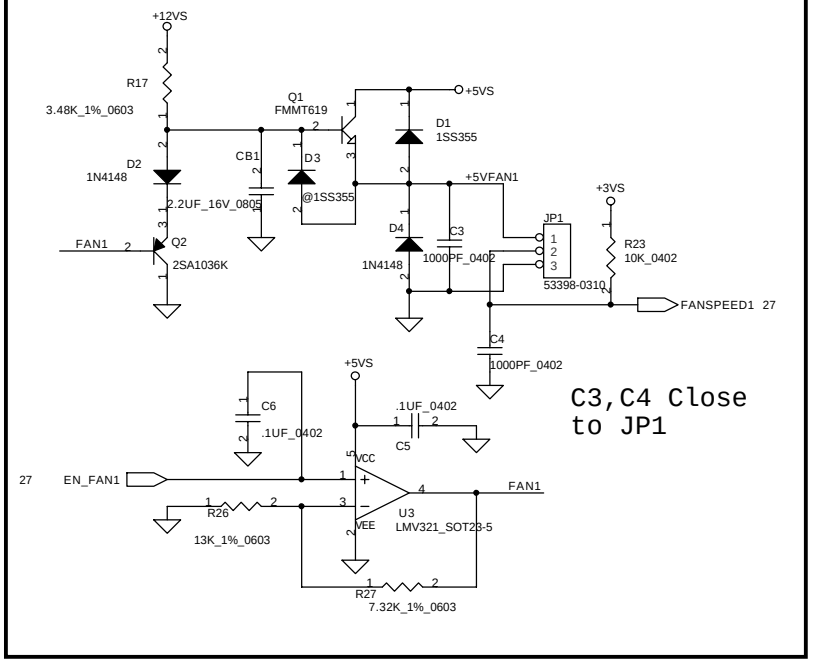


Thermal Sensor ADM1032AR



Fan Control circuit



C3,C4 Close to JP1

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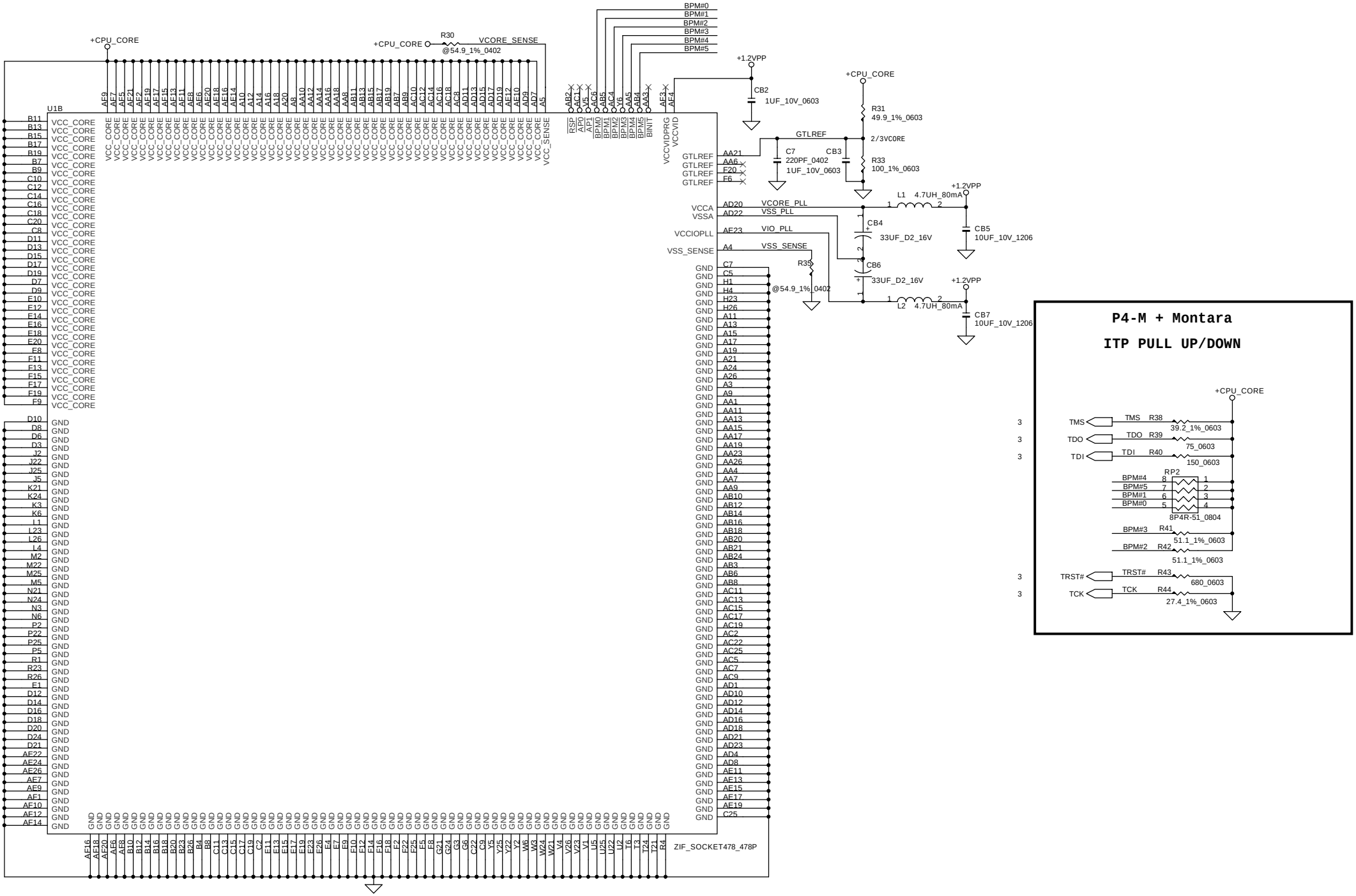

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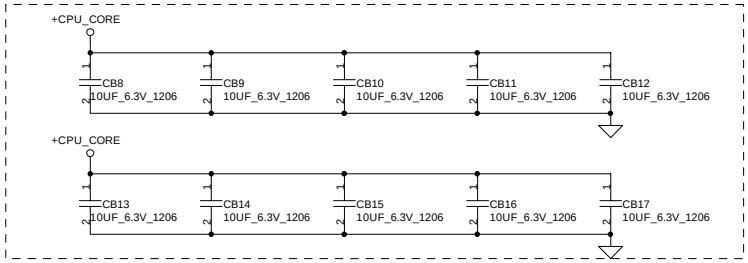
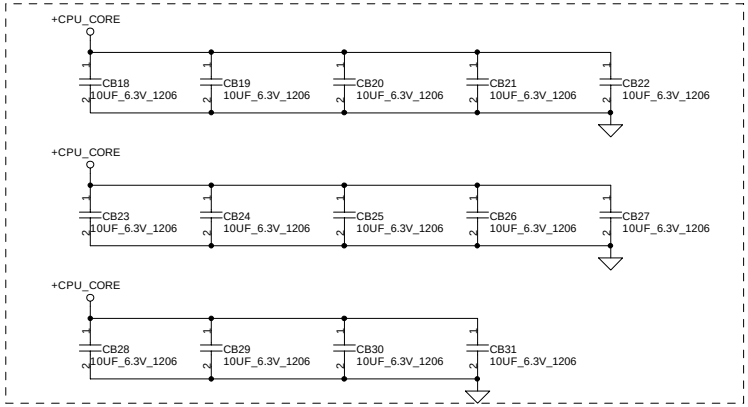
Layout note :

Place close to CPU, Use 2~3 vias per PAD.
Place .22uF caps underneath balls on solder side.
Place 10uF caps on the peripheral near balls.
Use 2~3 vias per PAD.

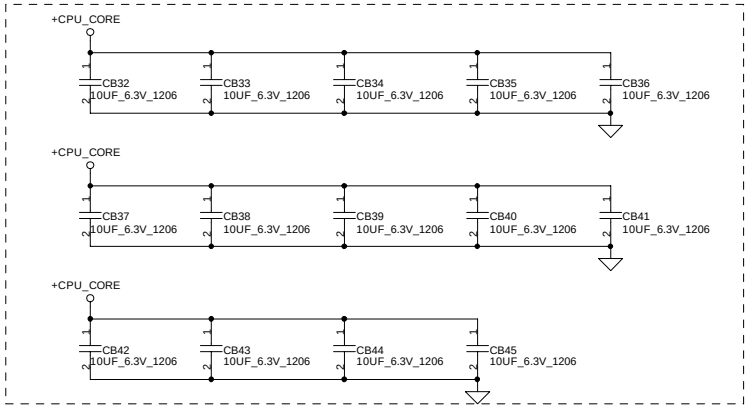
Please place these cap in the socket cavity area



Please place these cap on the socket north side



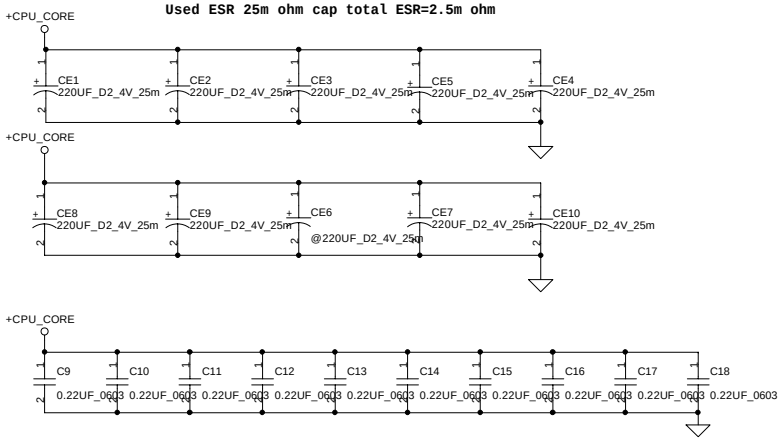
Please place these cap on the socket south side



Layout note :

Place close to CPU power and ground pin as possible (<1inch)

Used ESR 25m ohm cap total ESR=2.5m ohm



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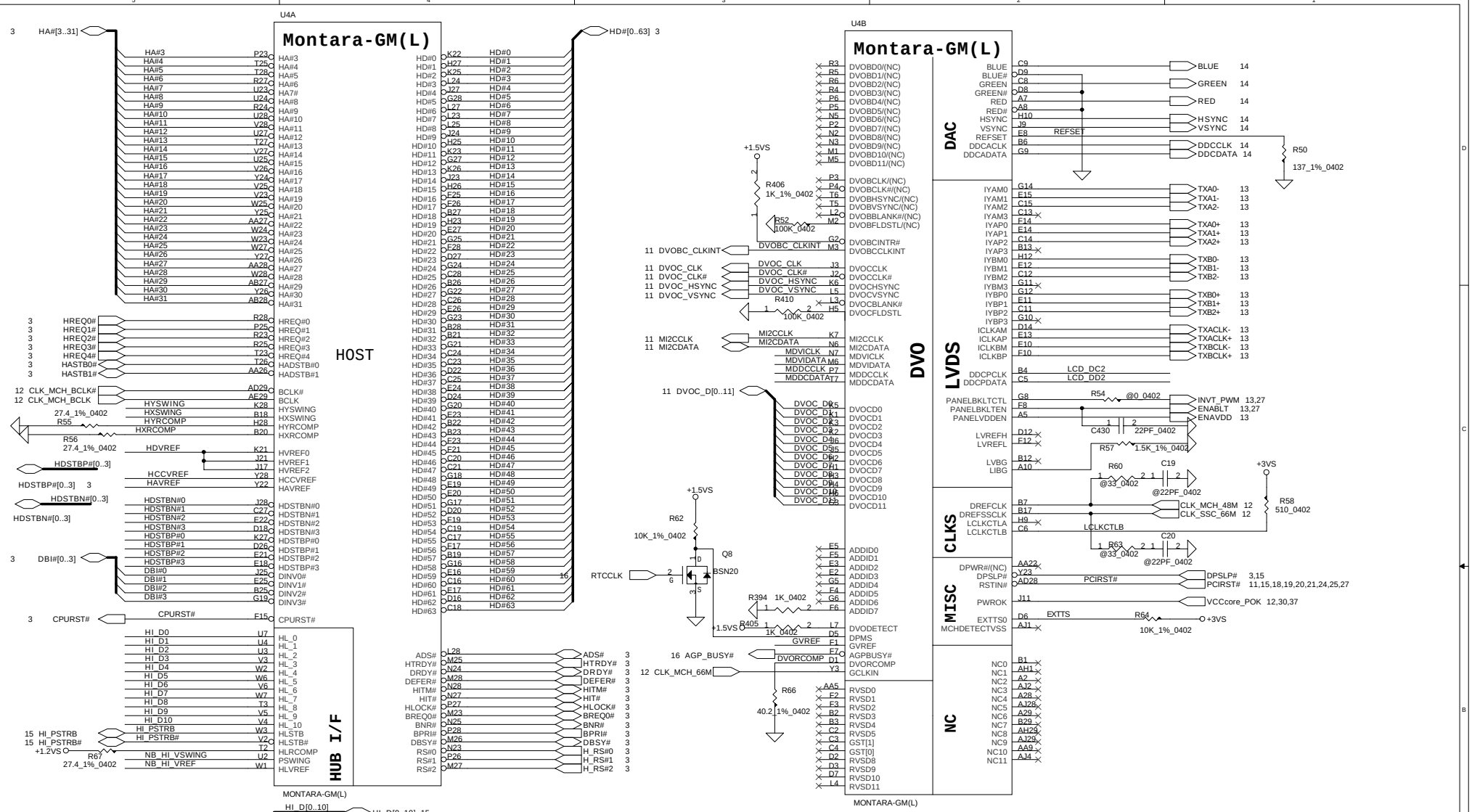
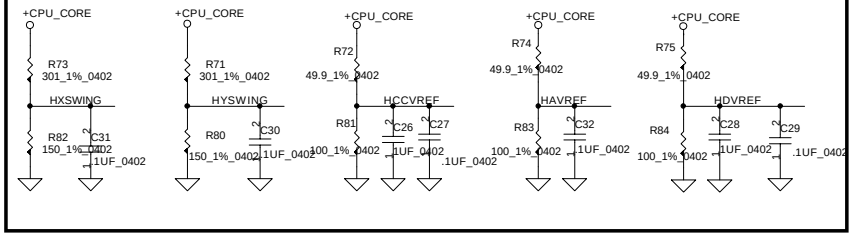
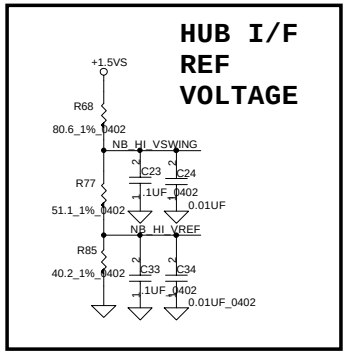


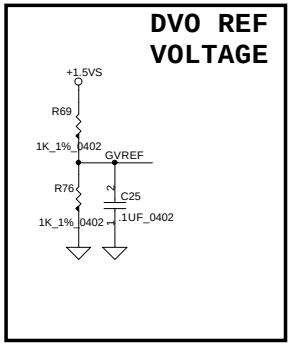
HOST REF VOLTAGE



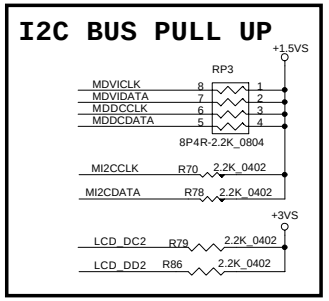
HUB I/F REF VOLTAGE



DVO REF VOLTAGE



I2C BUS PULL UP



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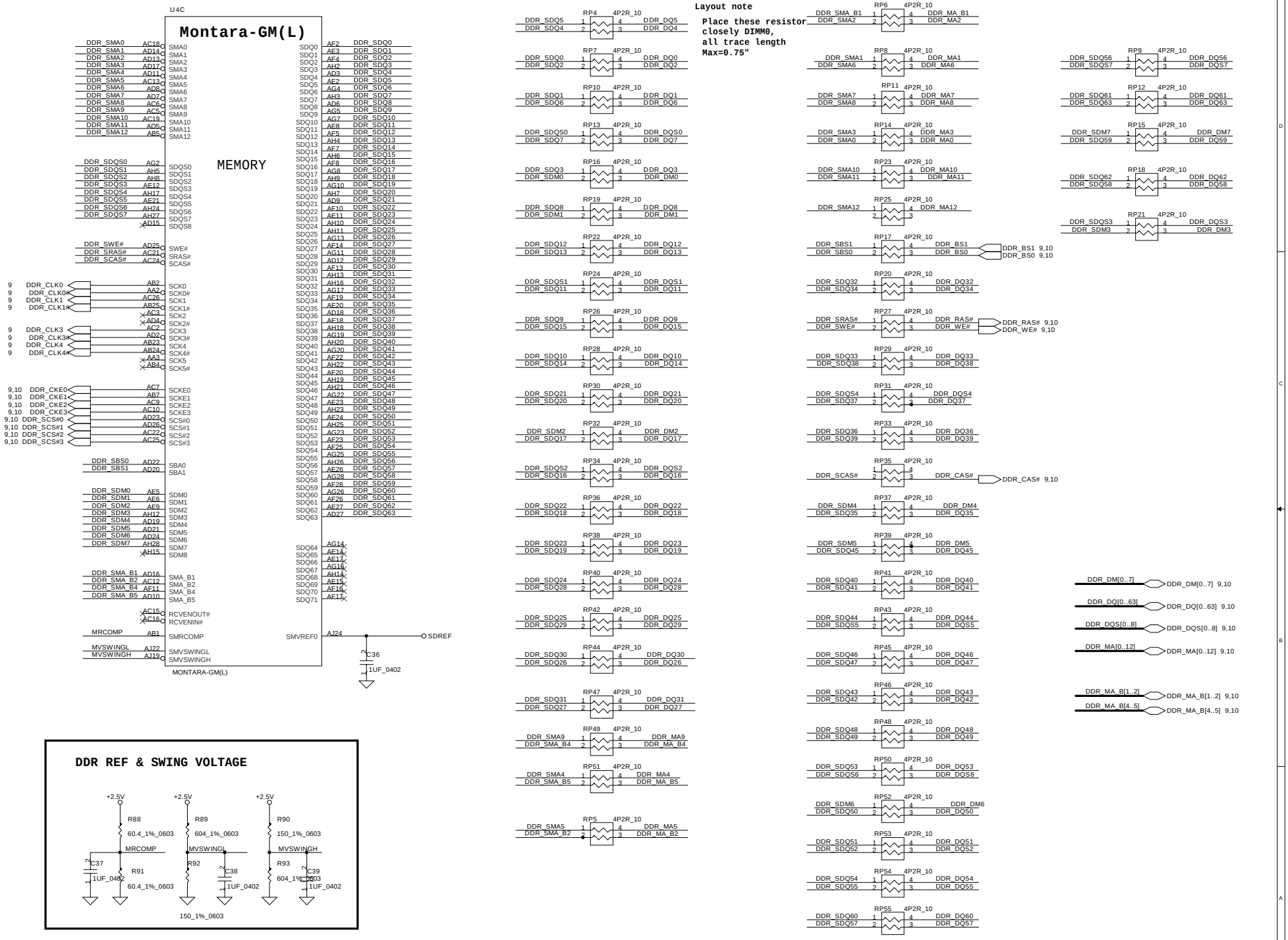

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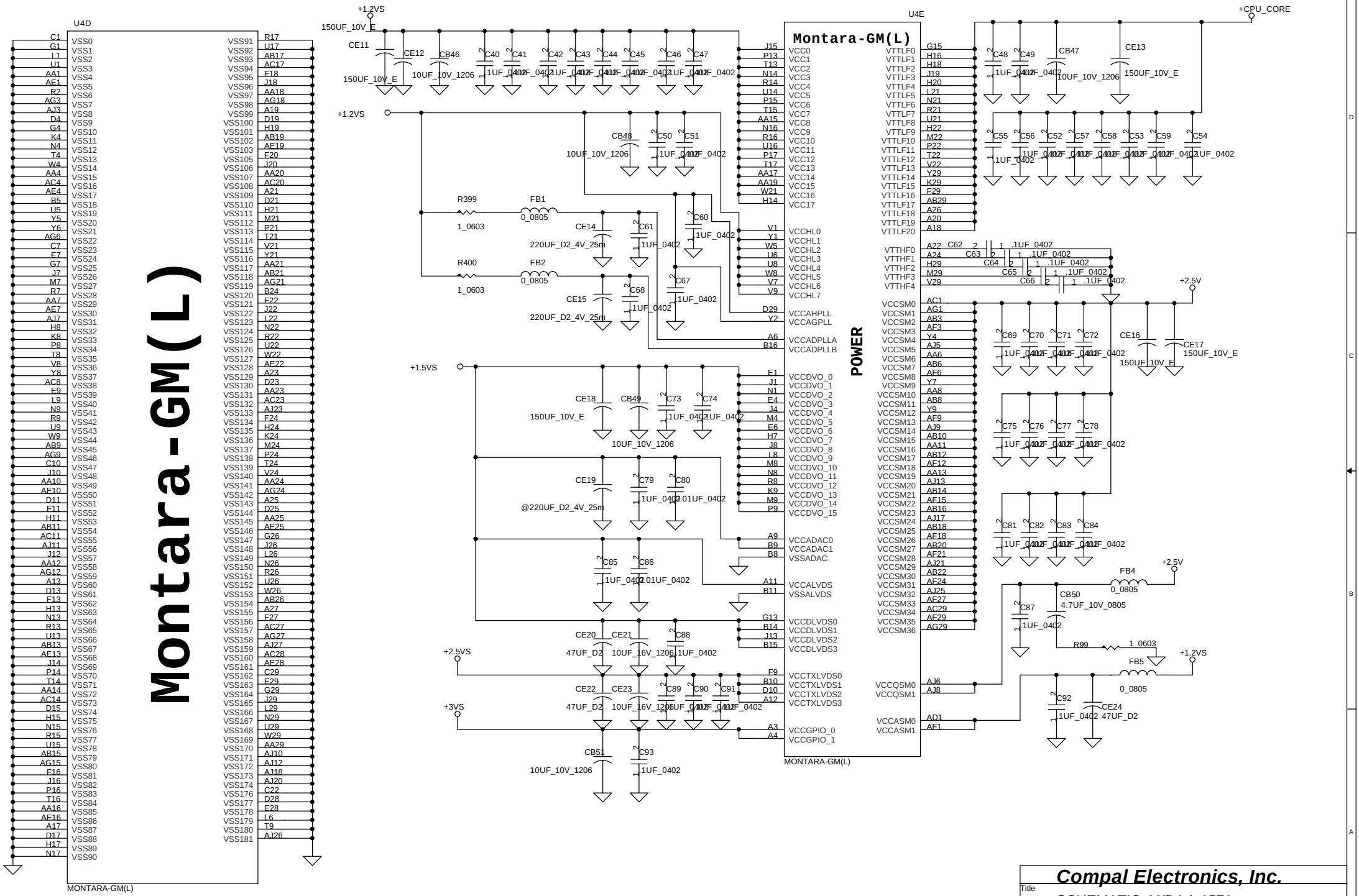

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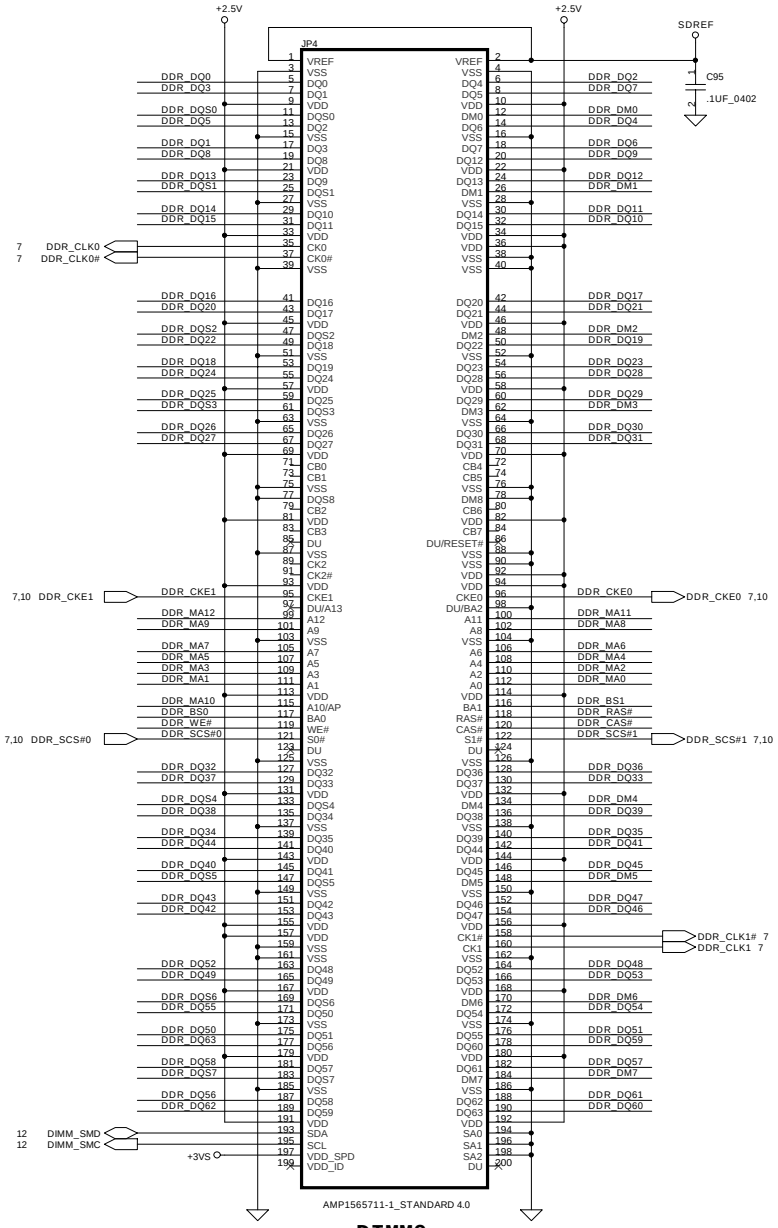
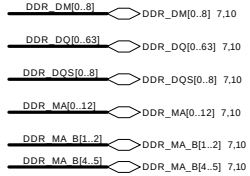
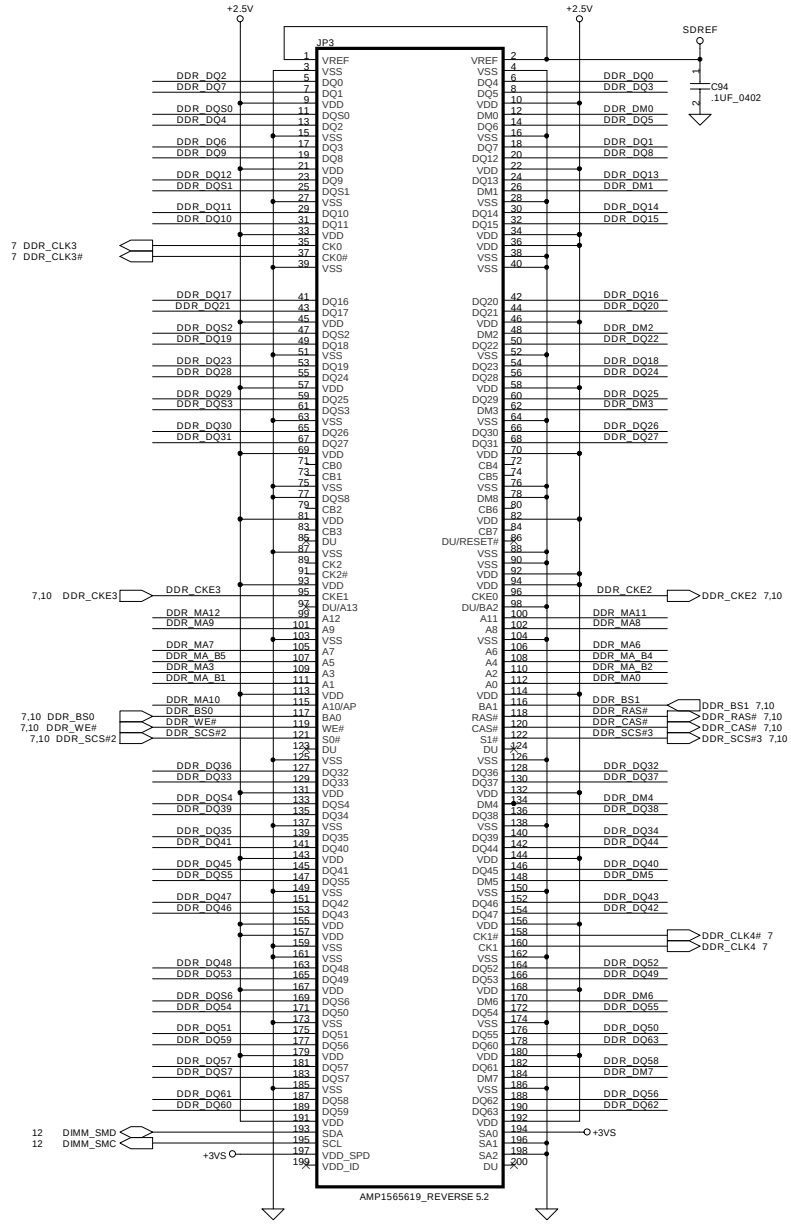


DIMM0

TOP SIDE





DIMM1

BOTTOM SIDE

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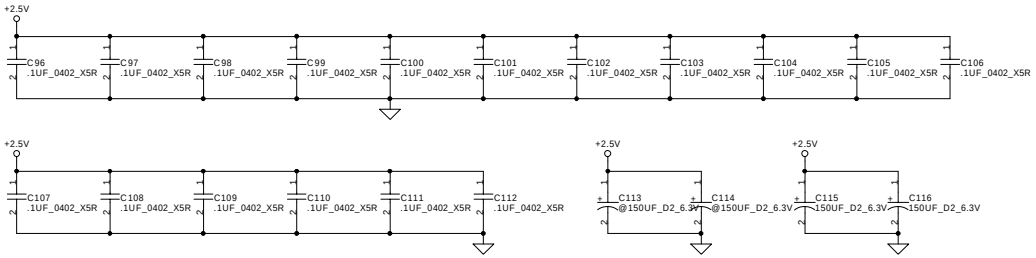
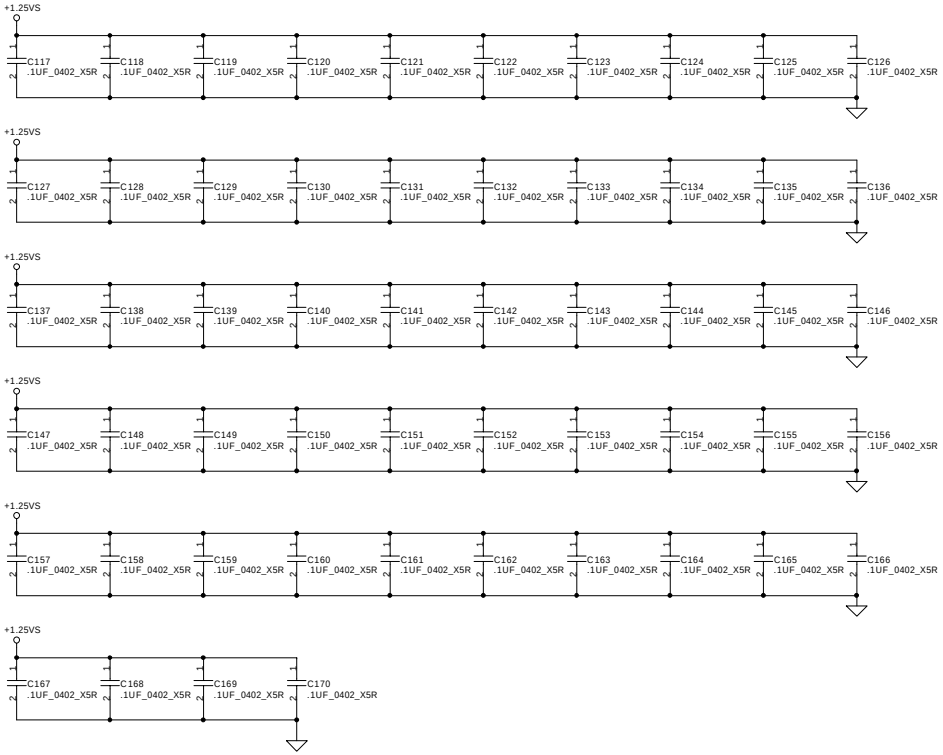
Layout note :

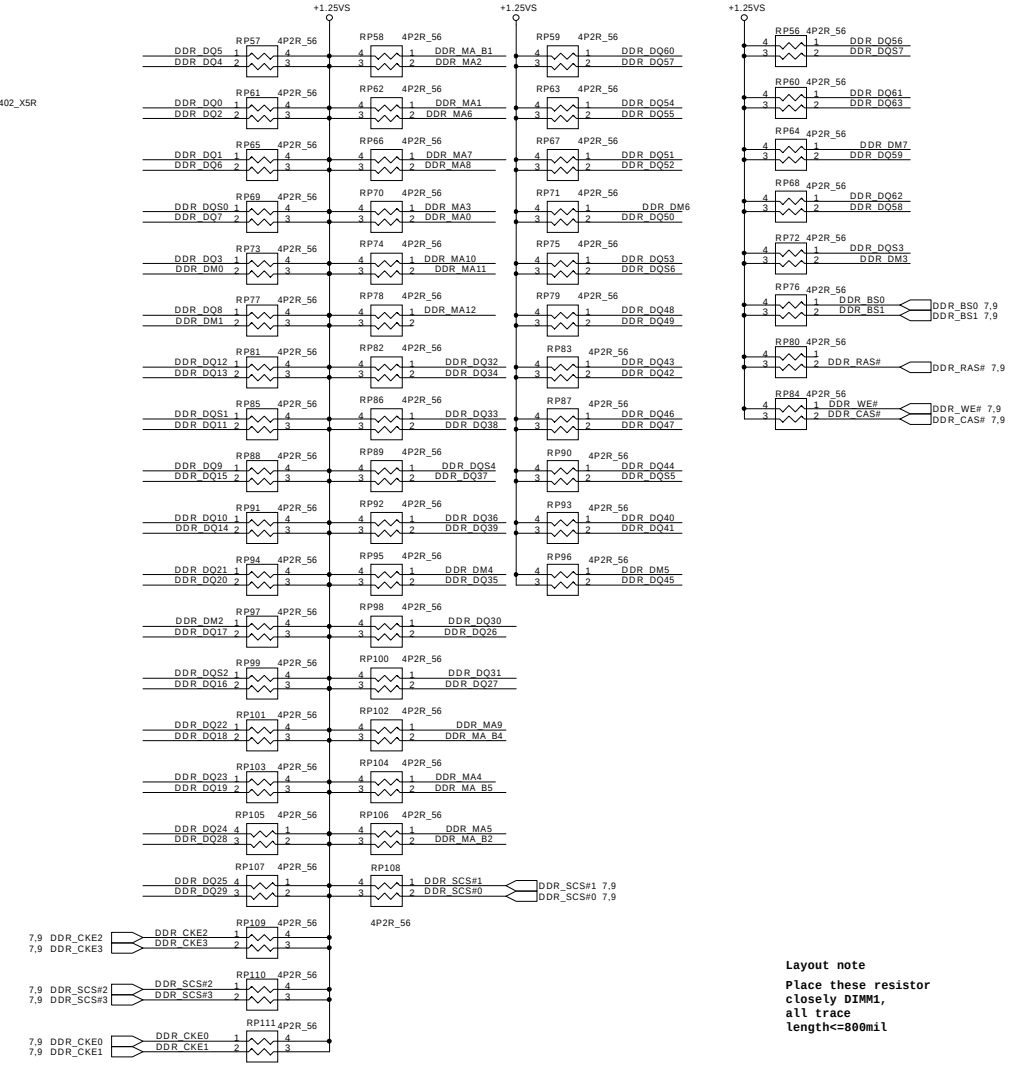
Distribute as close as possible to DDR-SODIMM.



Layout note :

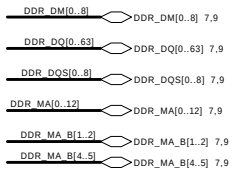
Place one cap close to every 2 pull up resistors termination to +1.25V





Layout note

Place these resistor closely DIMM1, all trace length<=800mil



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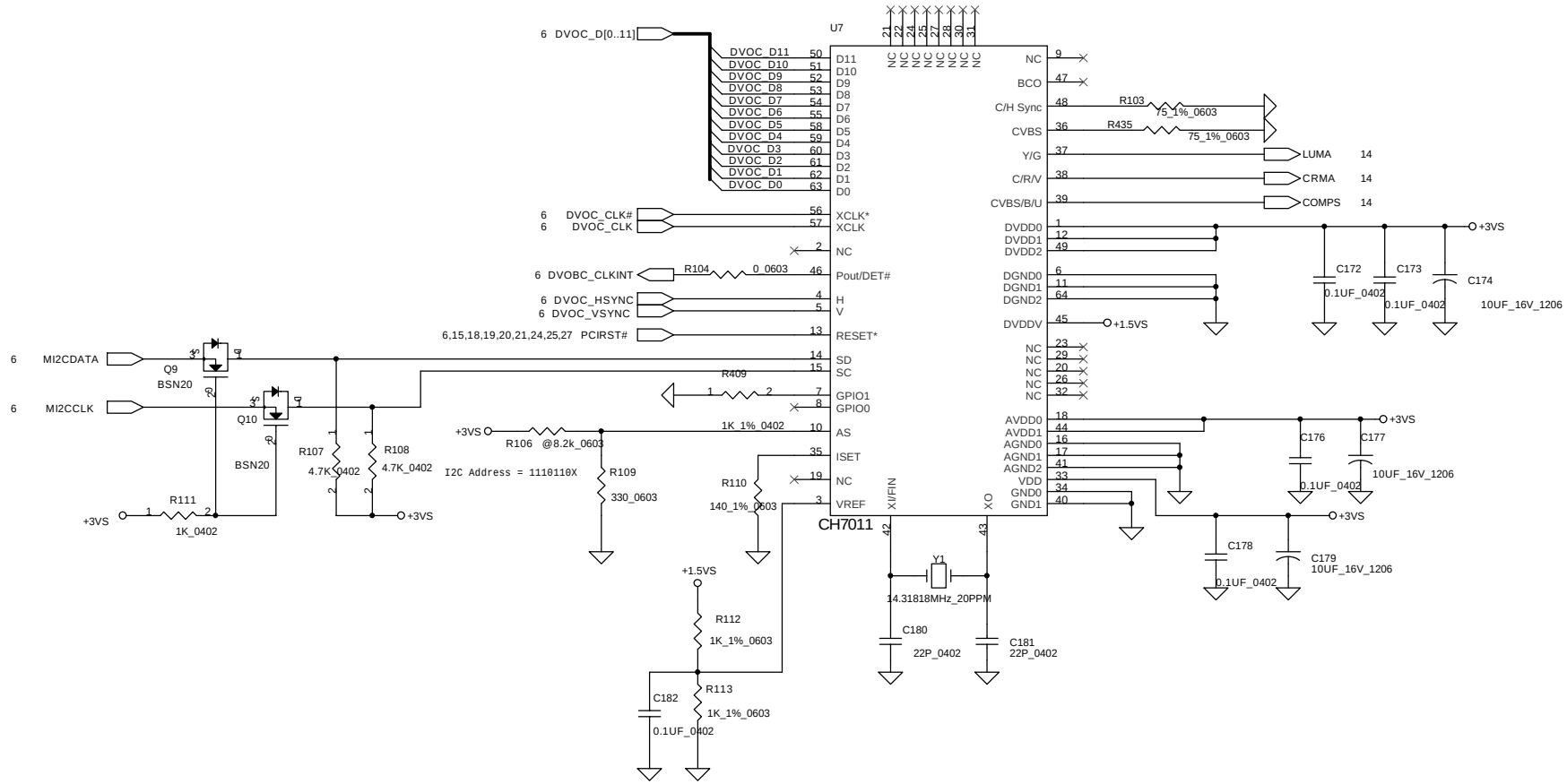

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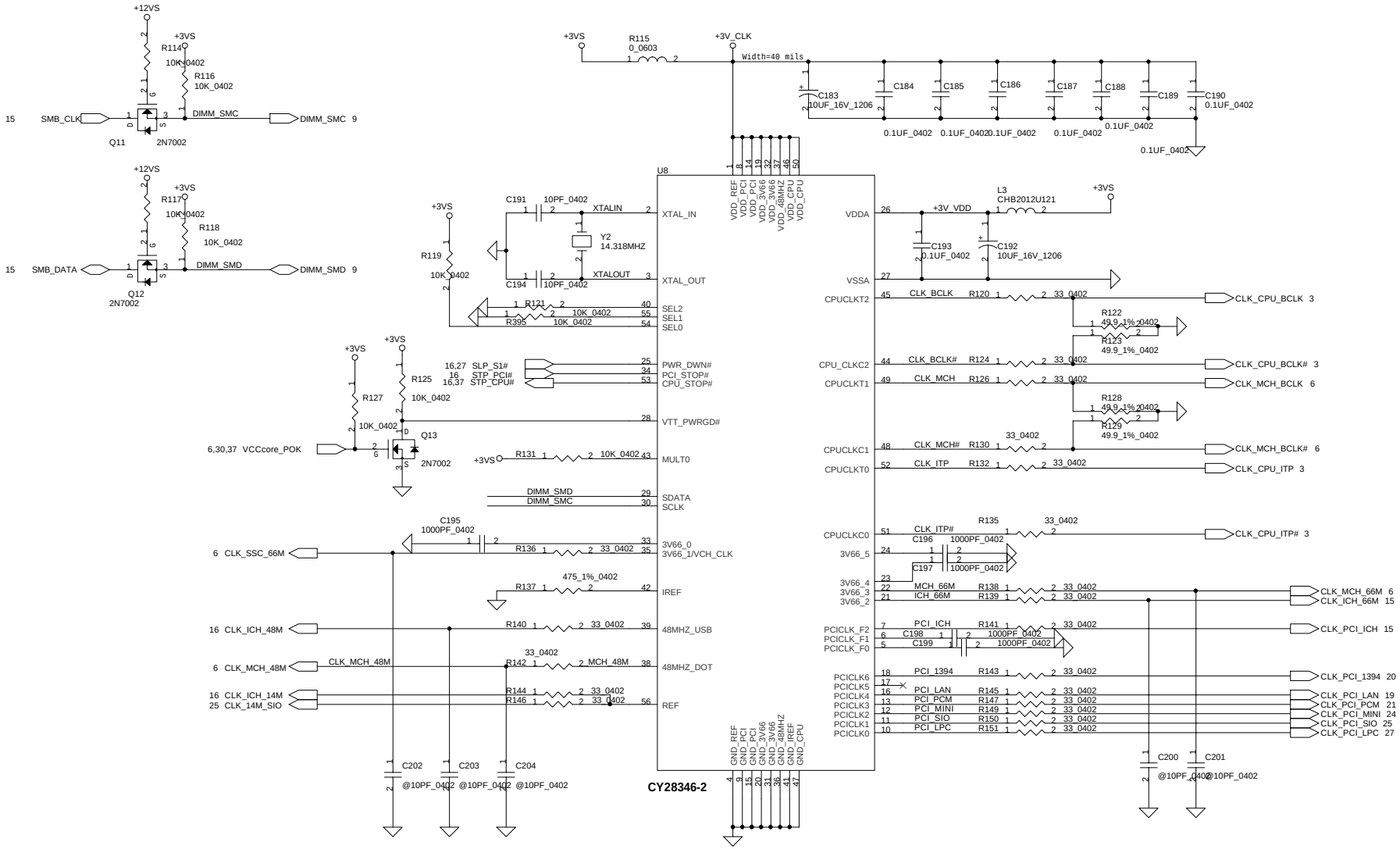
Clock Generator



SEL2	SEL1	SEL0	CPUCLKC[0..2]	CPUCLKT[0..2]
0	0	0	166.67	166.67
0	0	1	100.00	100.00
0	1	0	200.00	200.00
0	1	1	133.33	133.33

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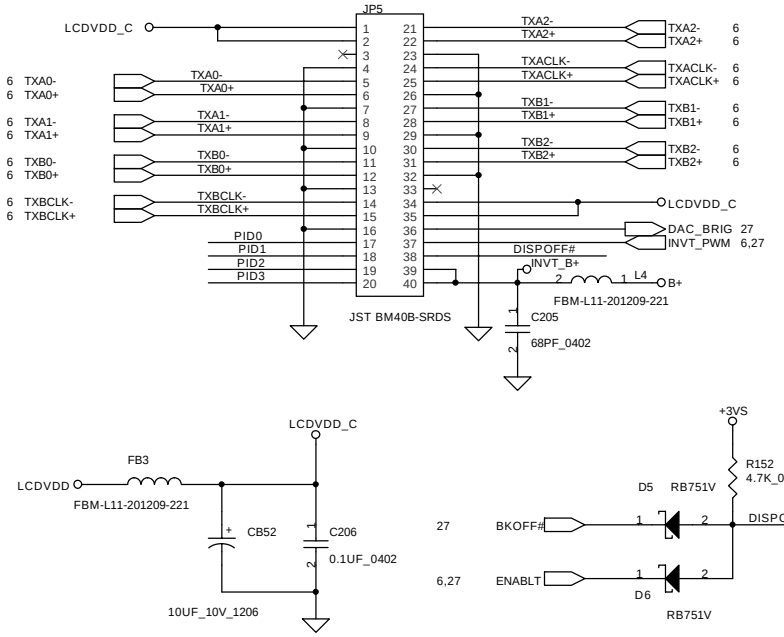
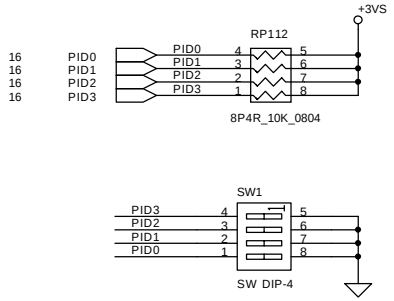
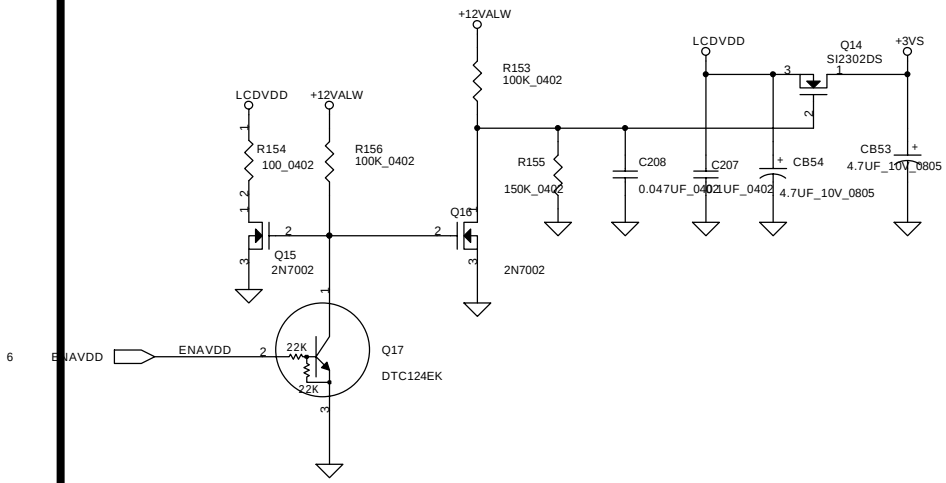
LCD CONN



PANEL ID switch



LCD POWER CIRCUIT



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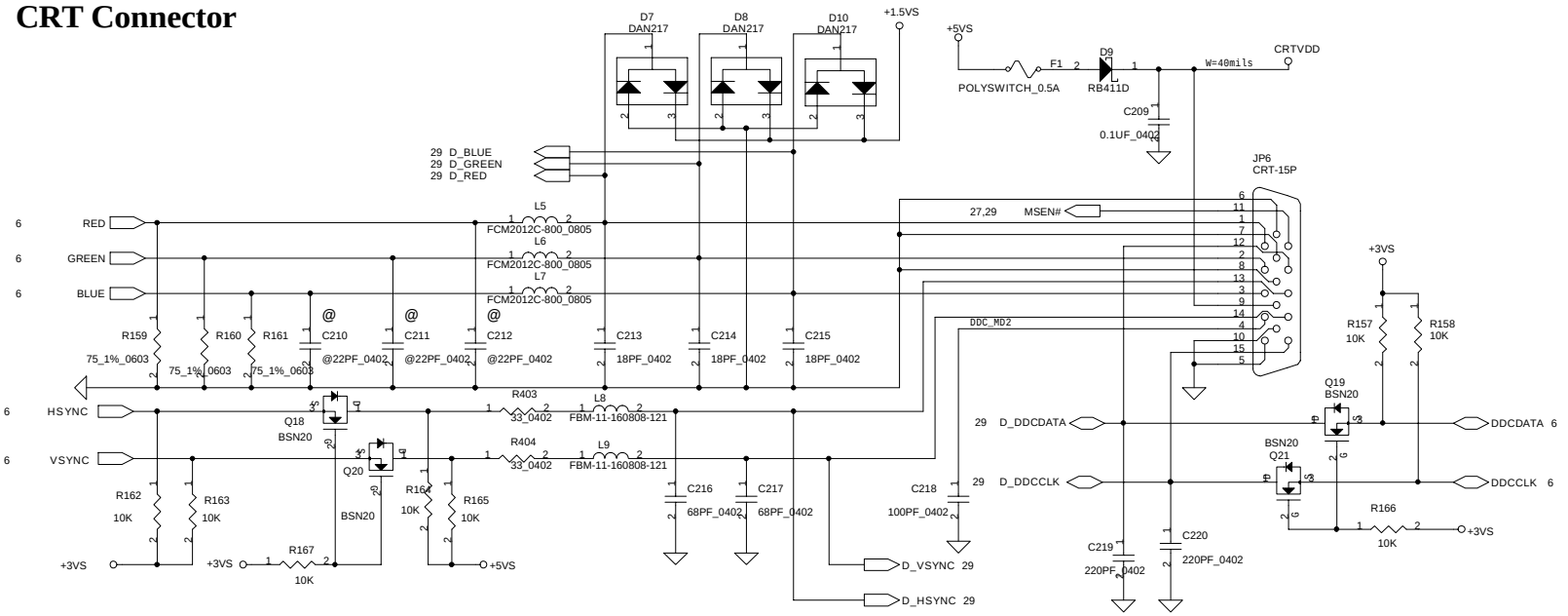
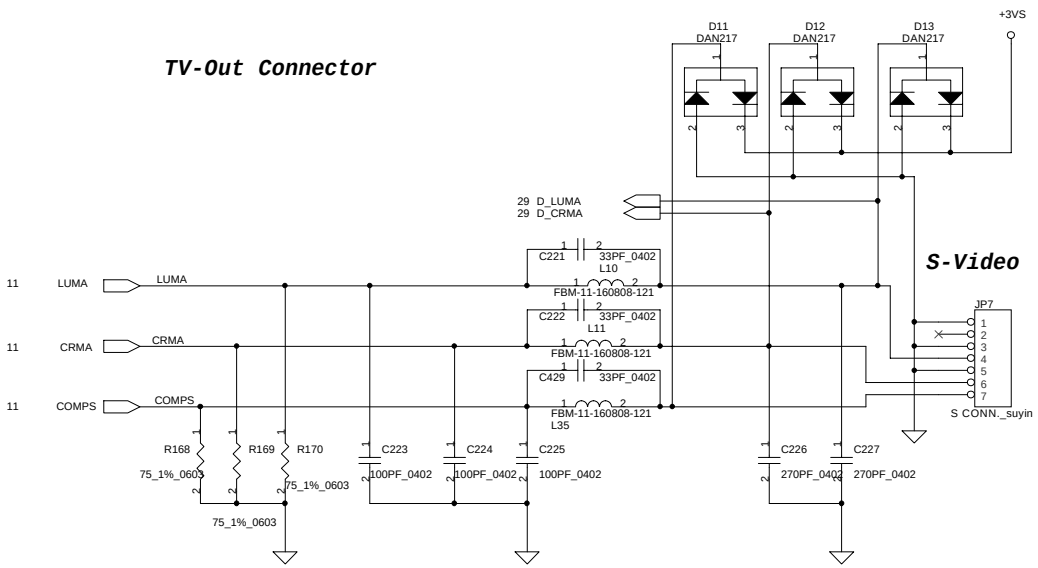
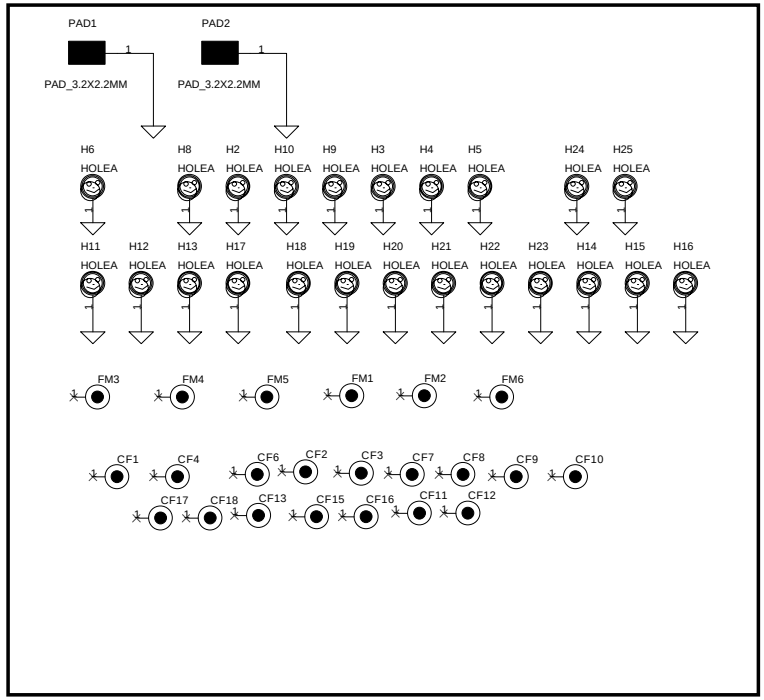
CRT Connector



TV-Out Connector





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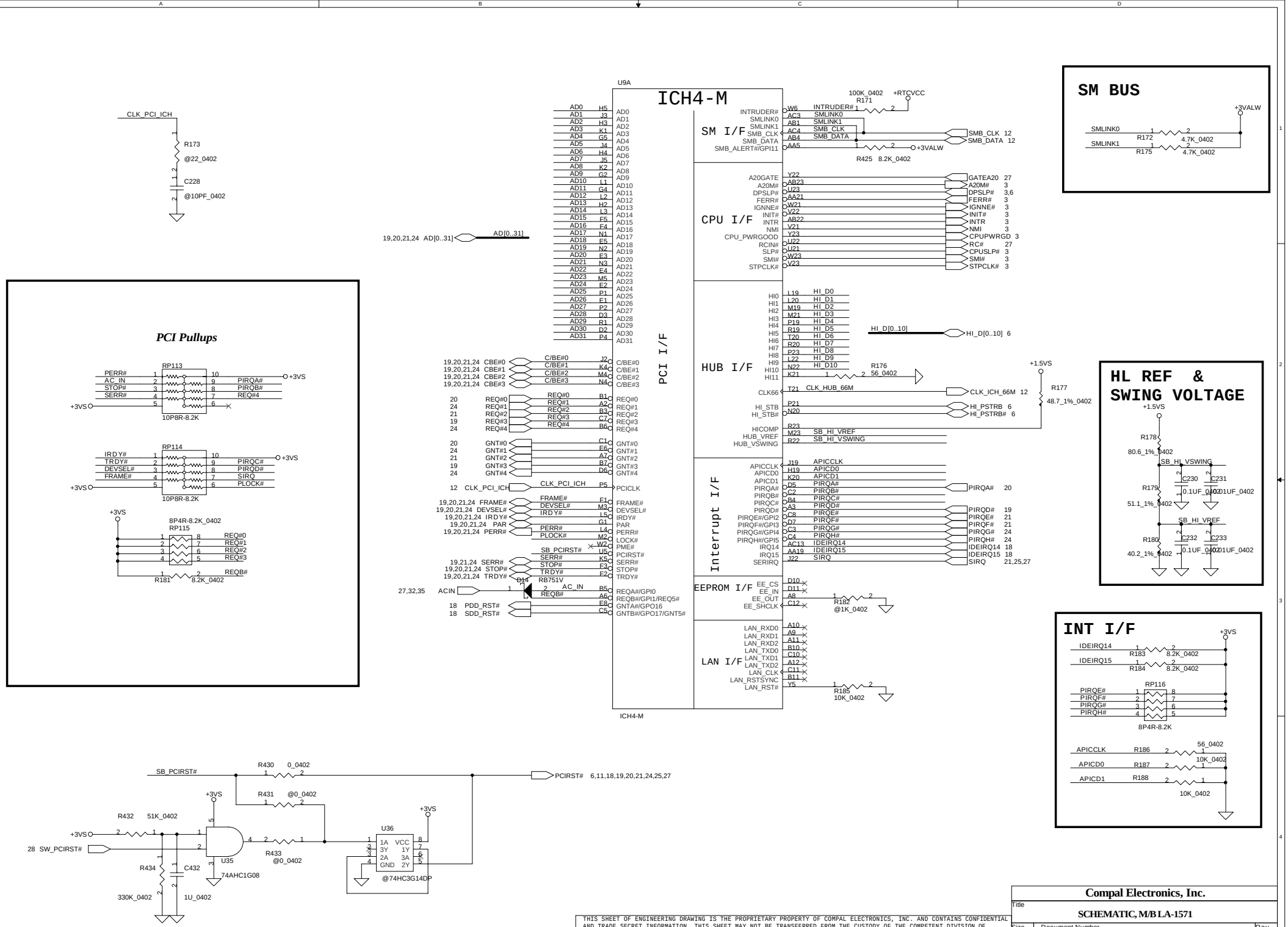

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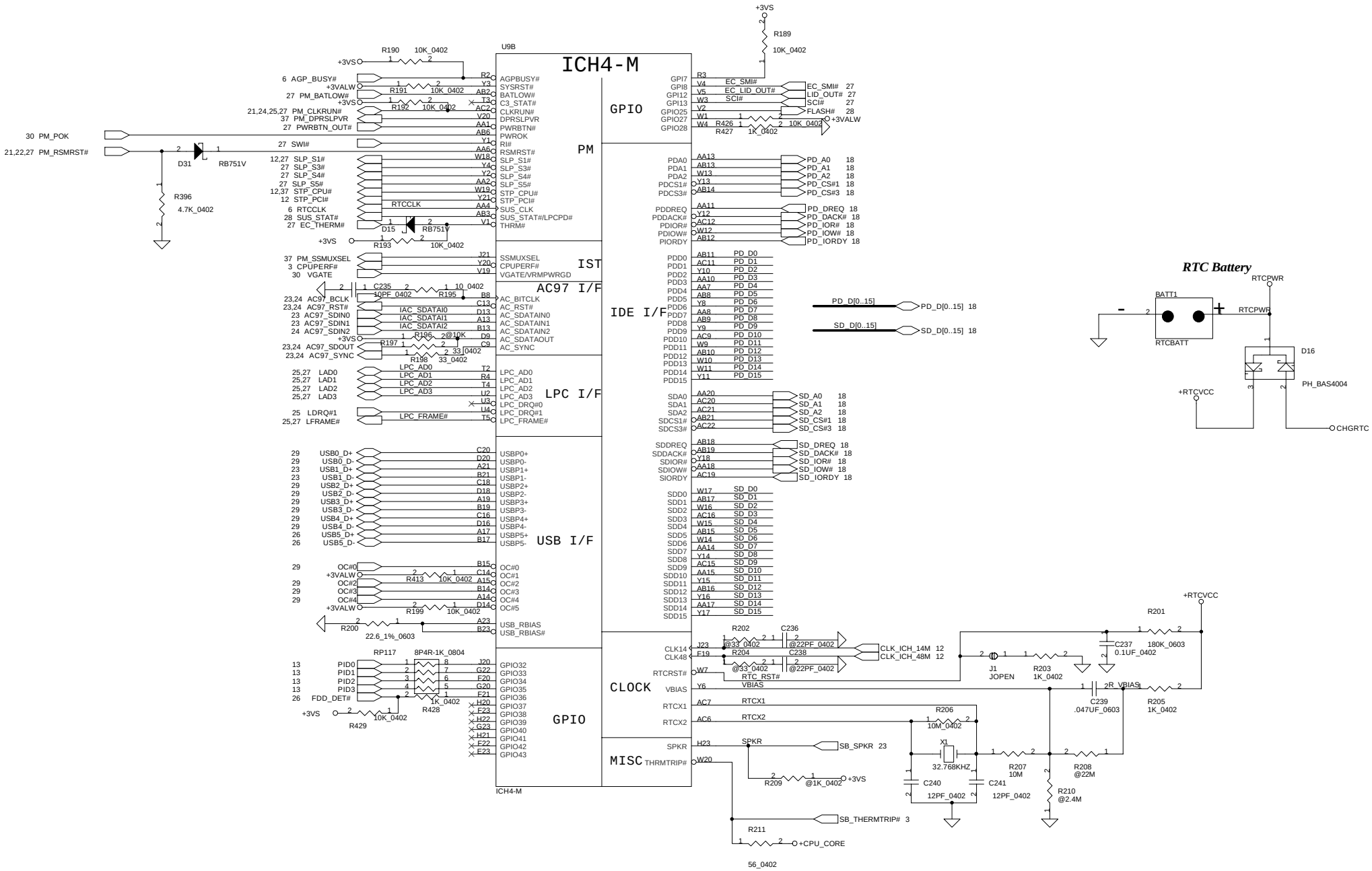

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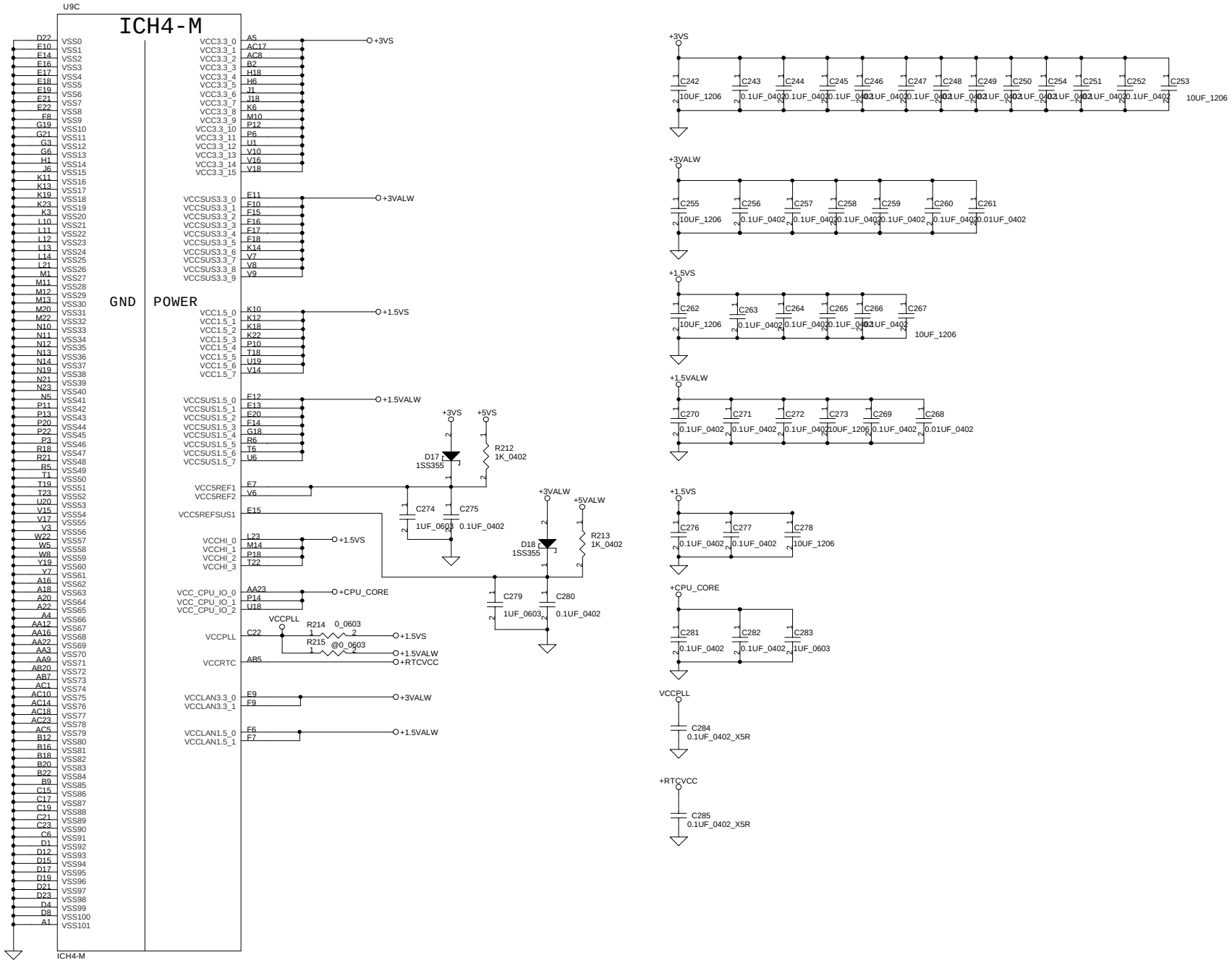

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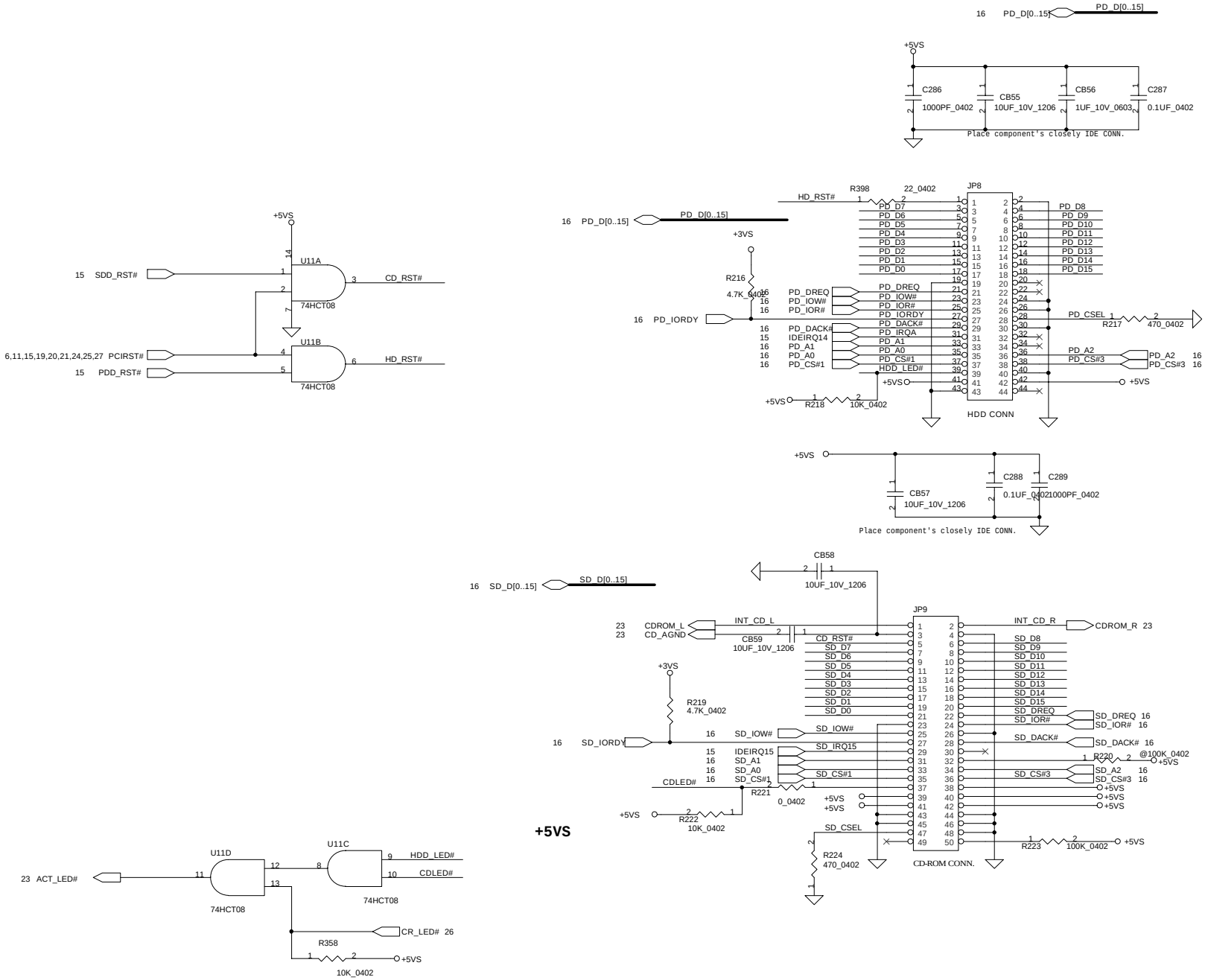
HDD/CD-ROM Module



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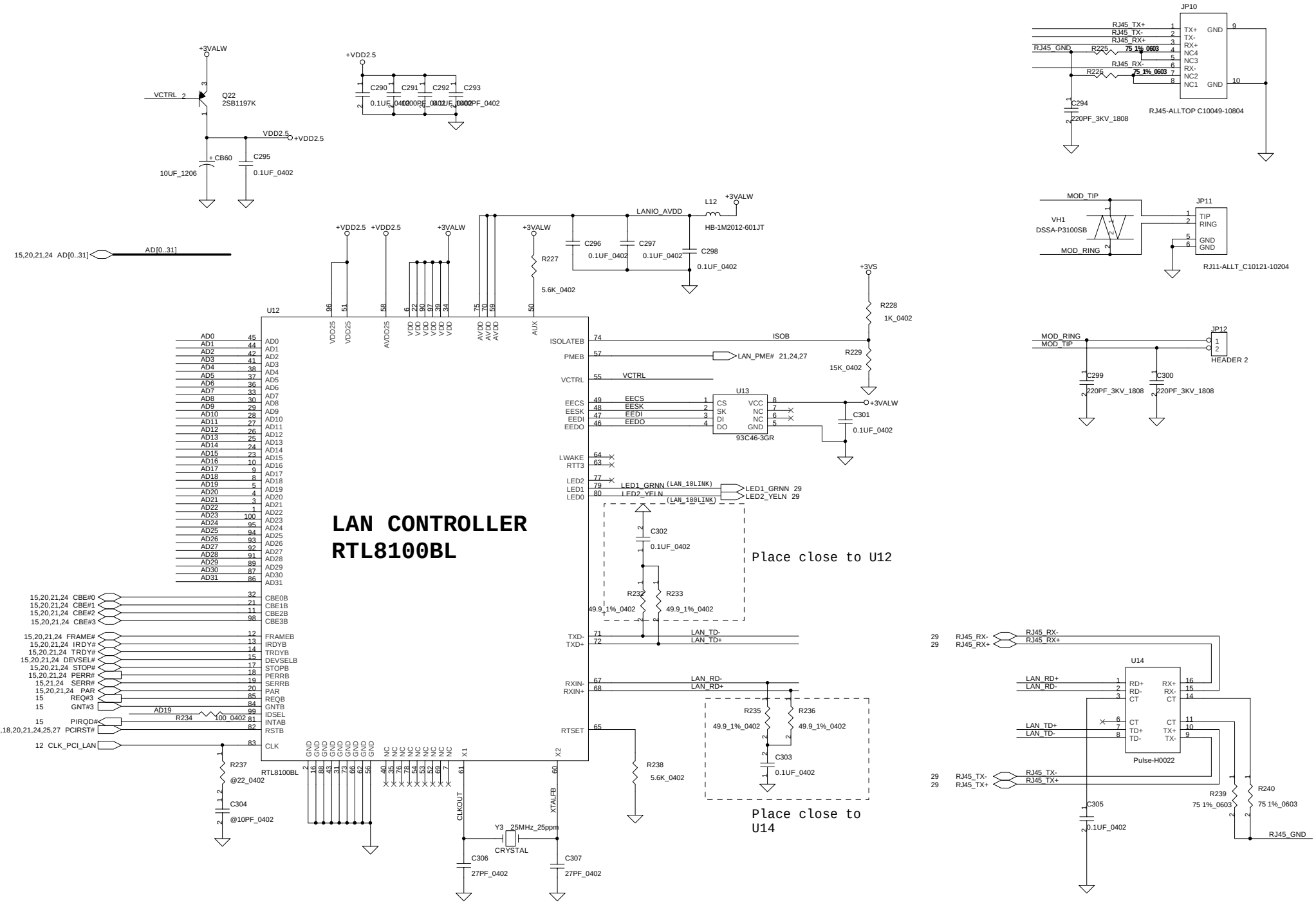

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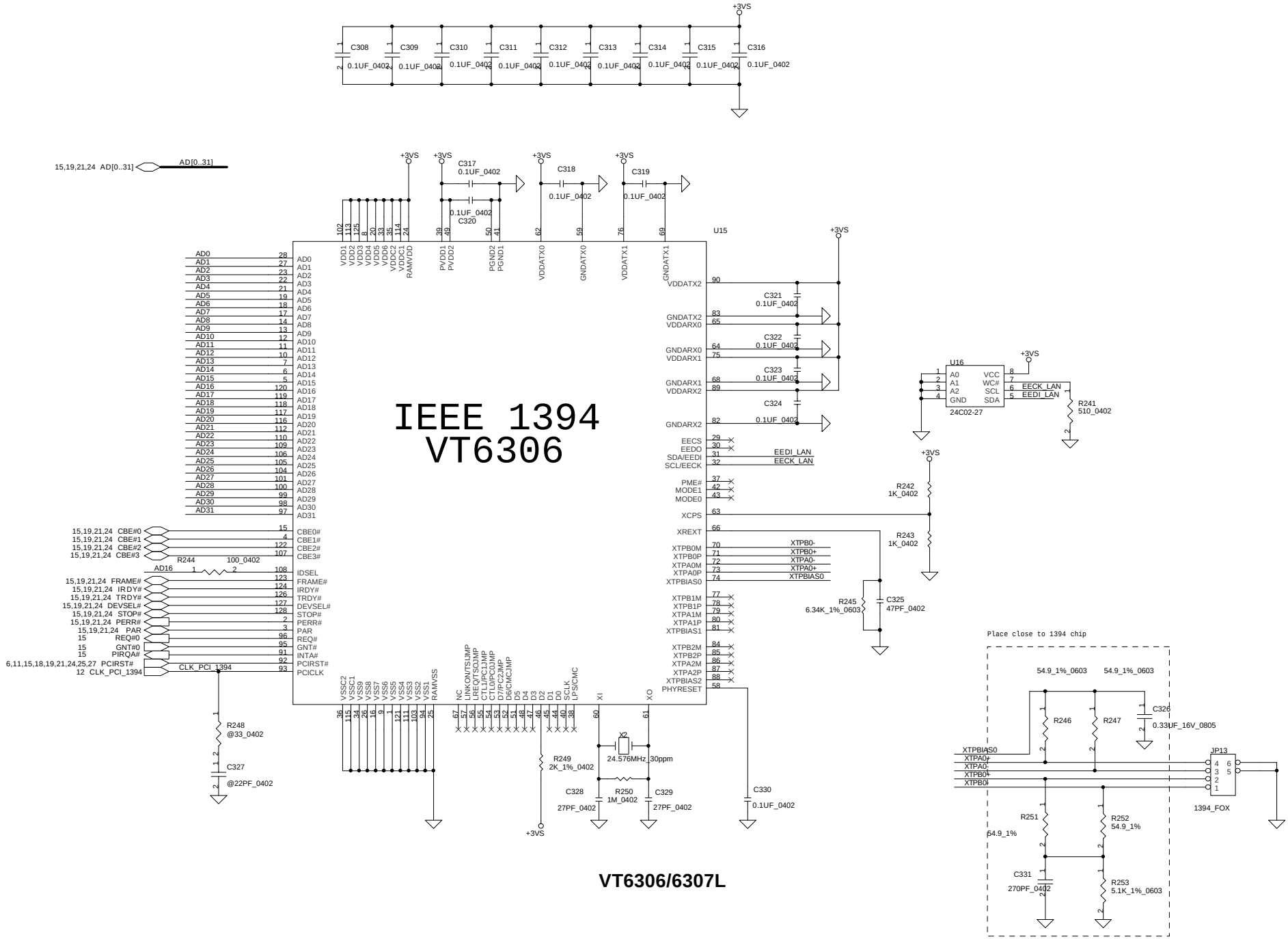
IEEE1394 Controller/PHY



VT6306/6307L

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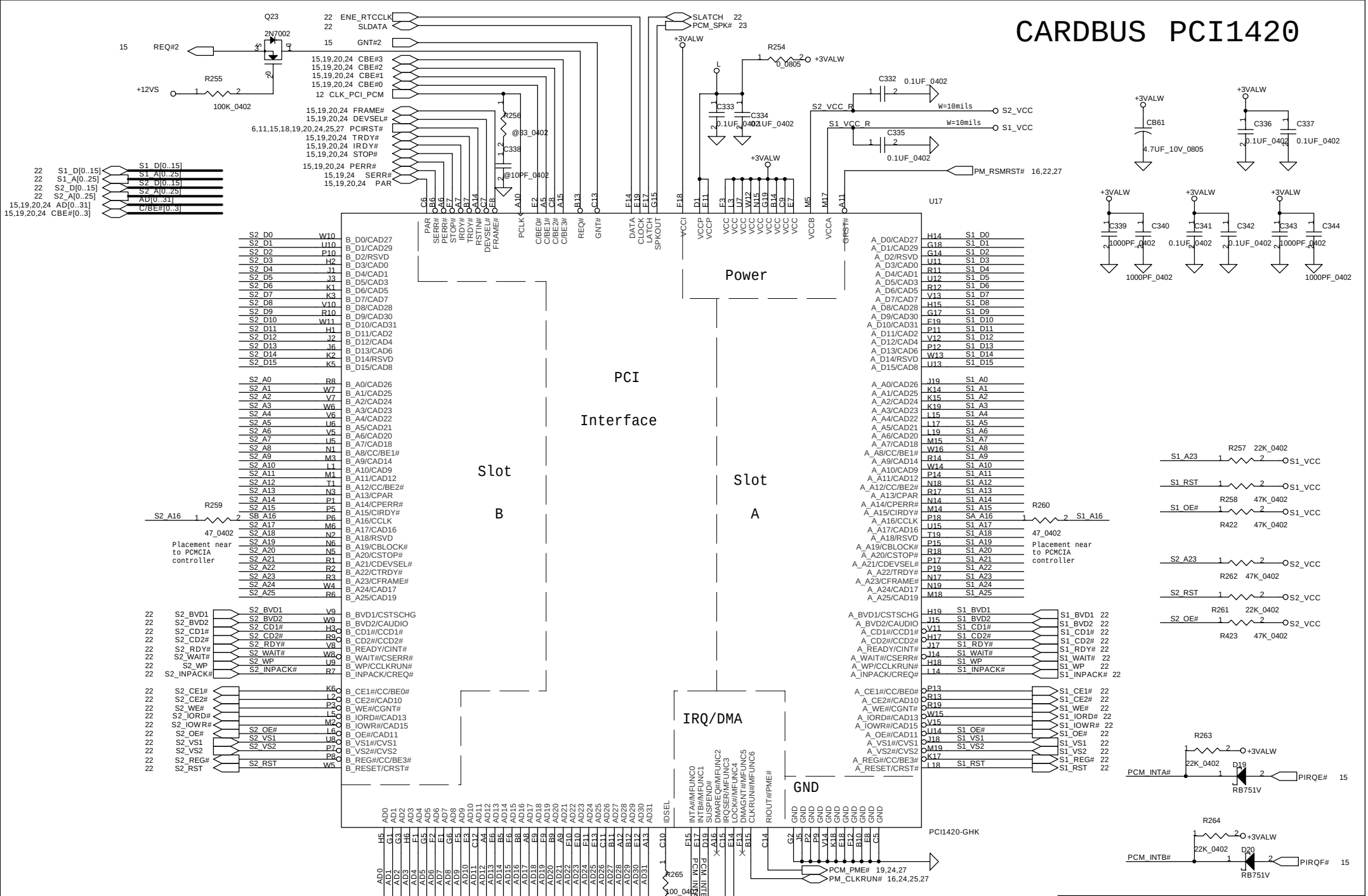
CARDBUS PCI1420



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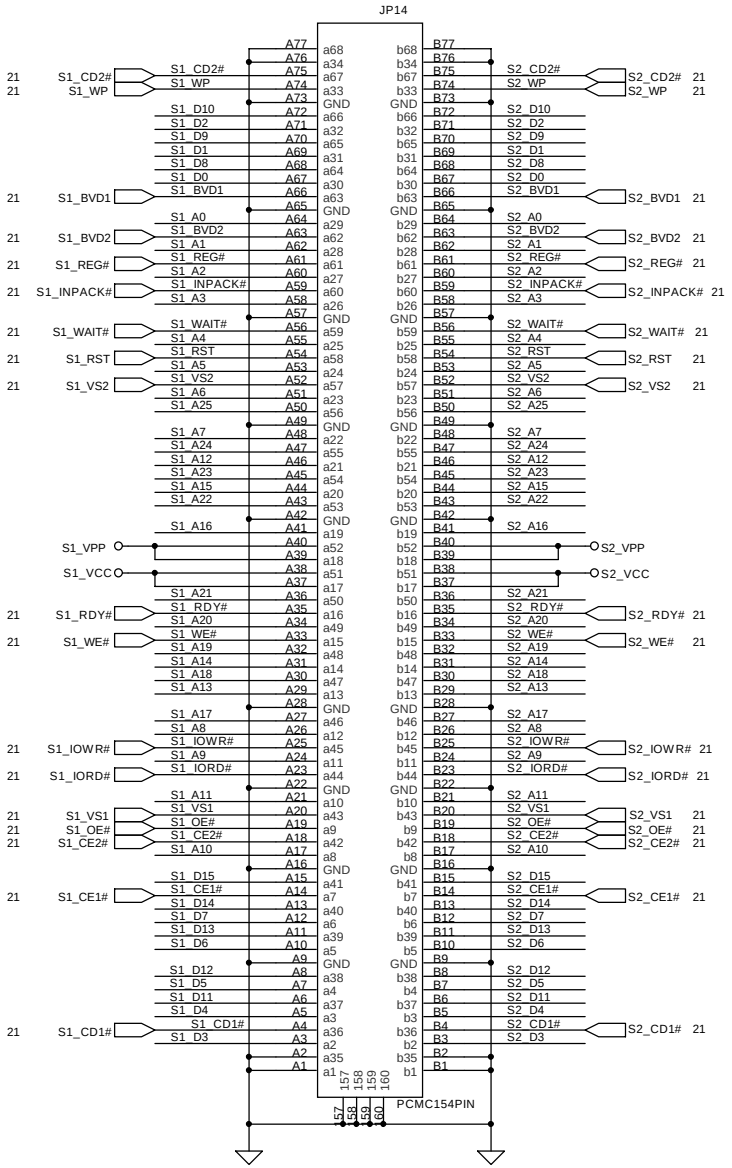
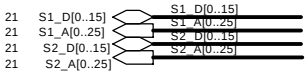
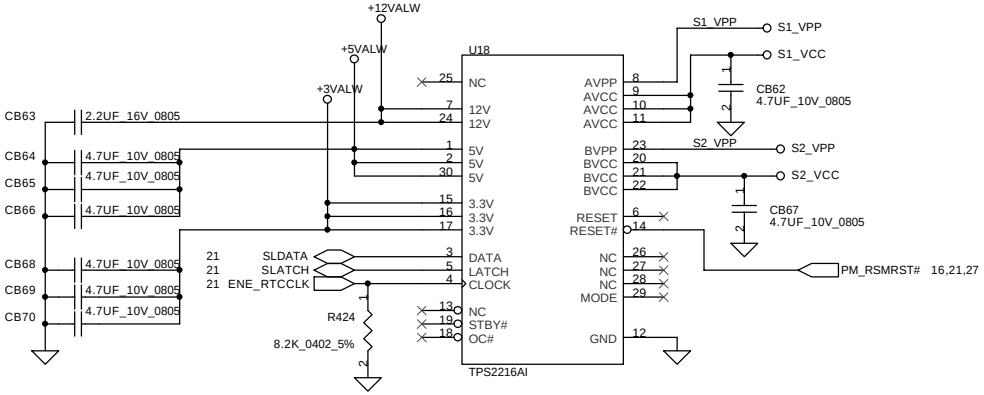
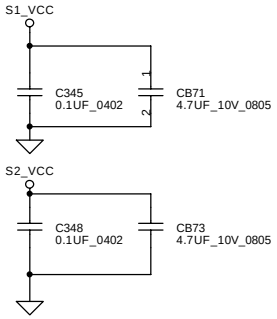
CARDBUS SOCKET

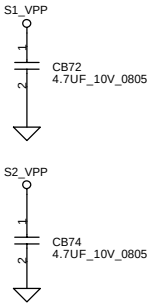




PCMCIA POWER CTRL.







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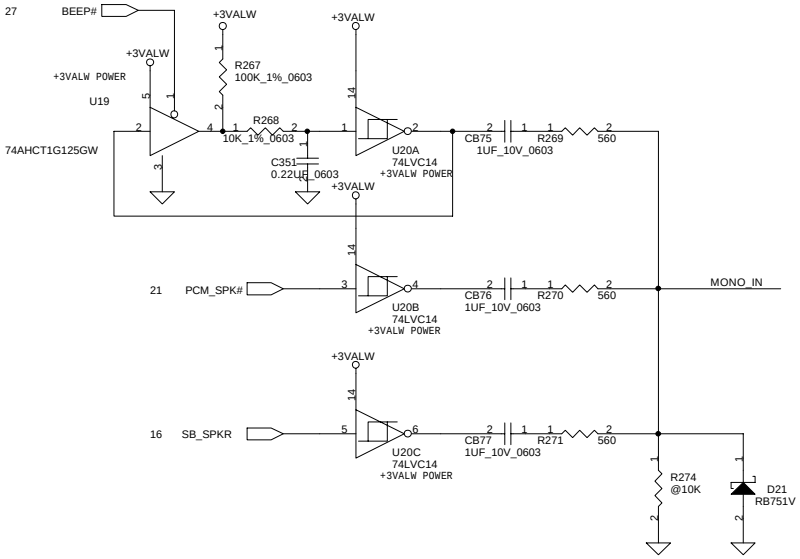
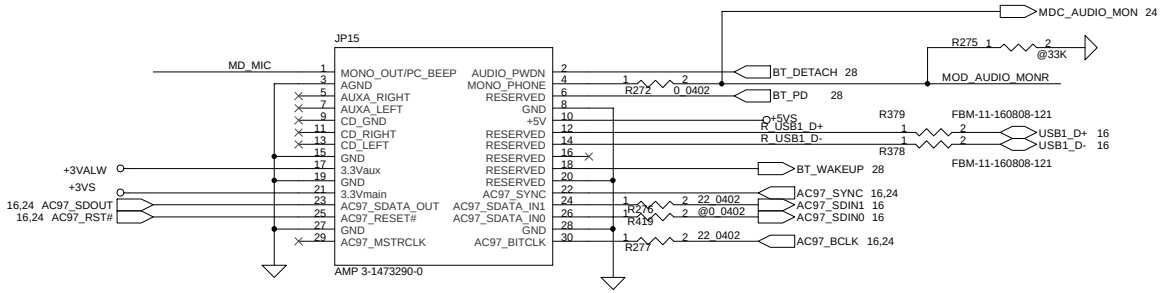
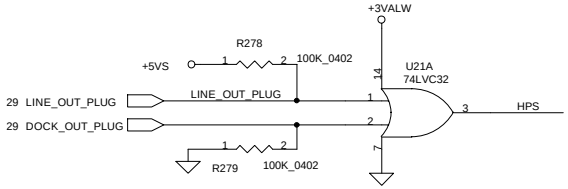
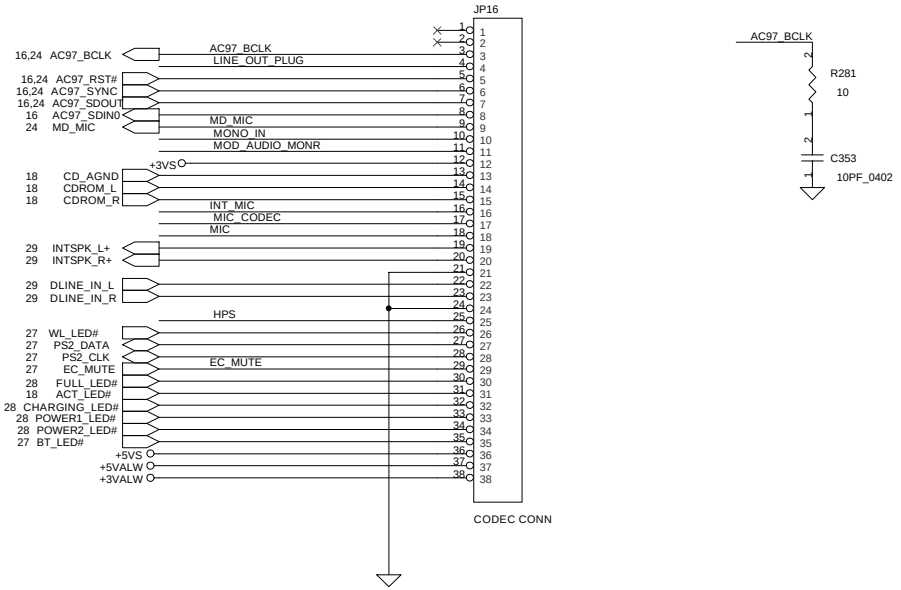


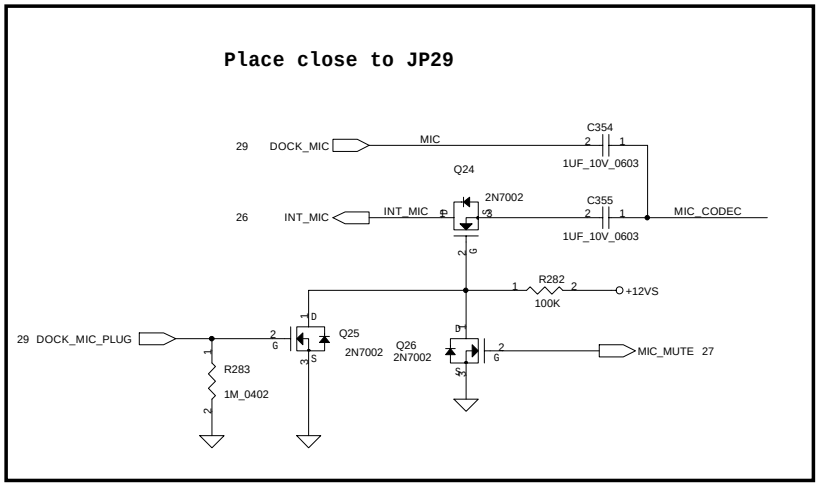
BT/MDC CONN





AC97 CODEC ALC202 CONN





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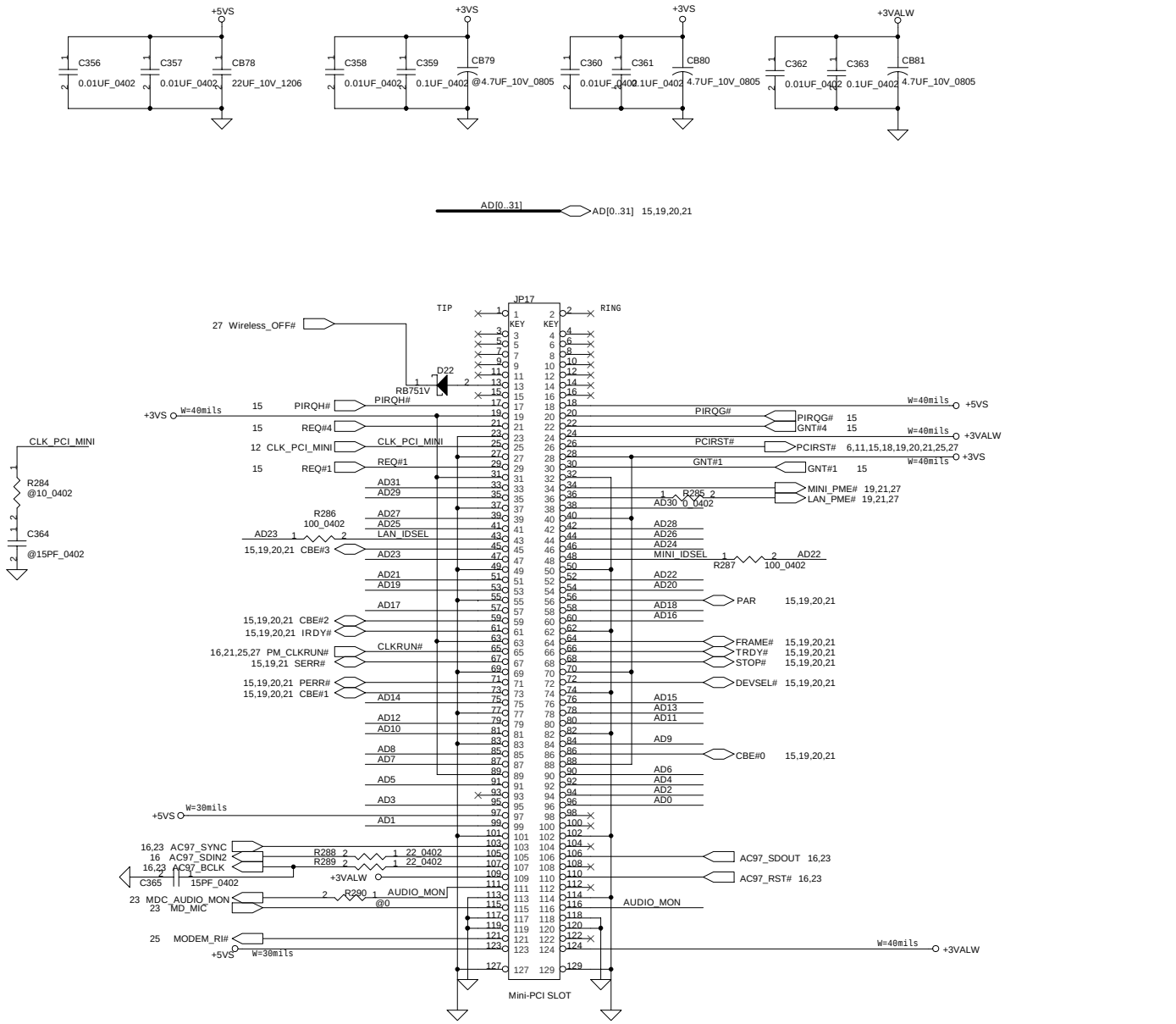
Mini-PCI Slot



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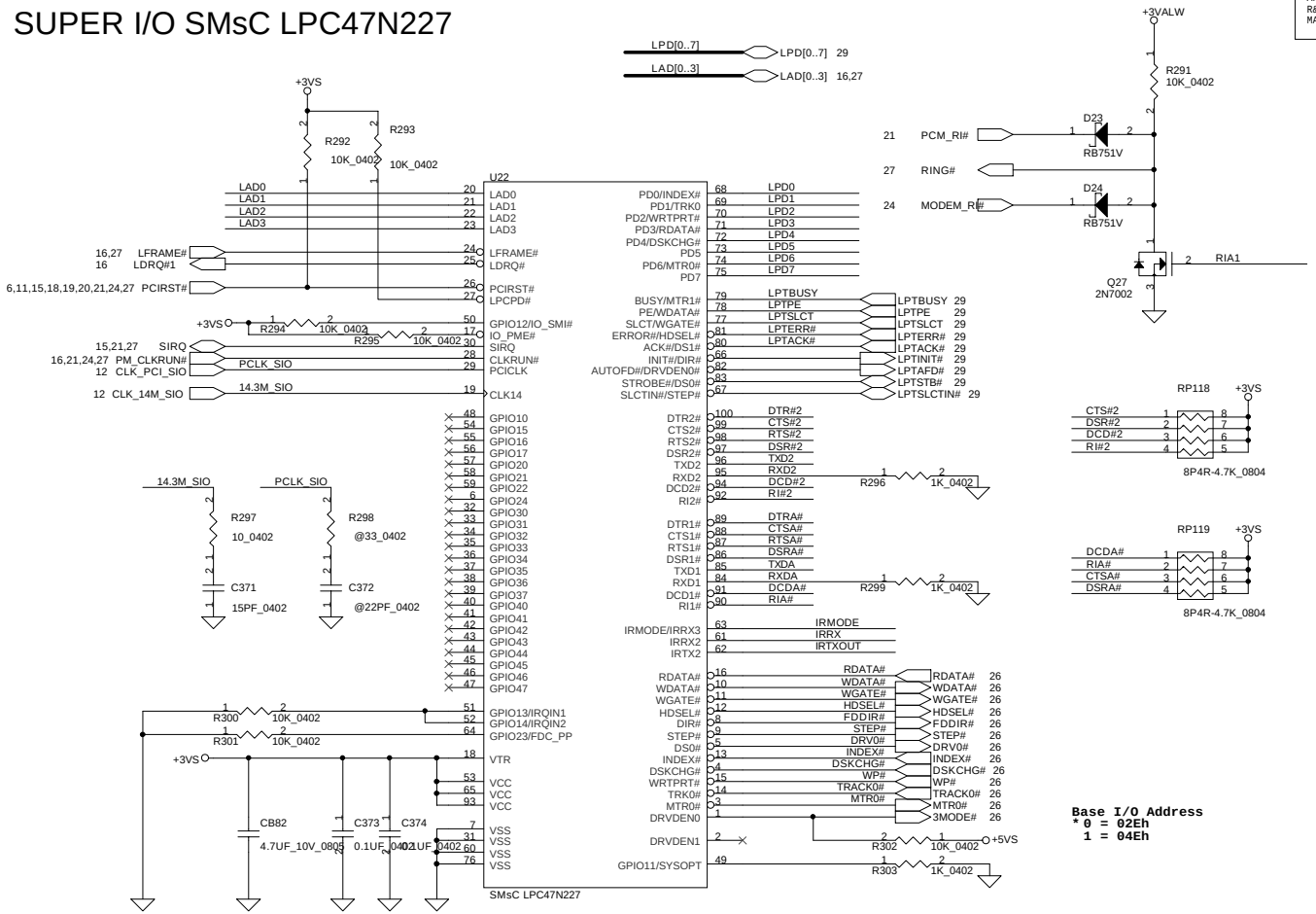
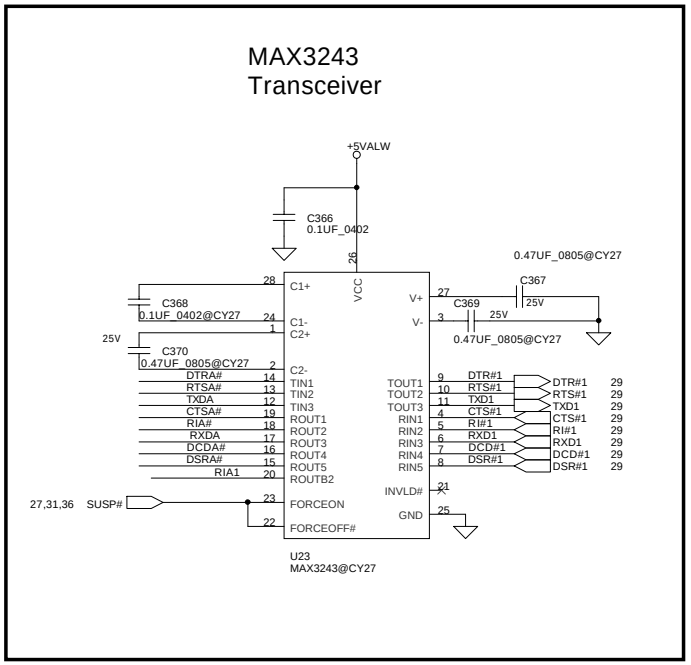
SUPER I/O SMsC LPC47N227

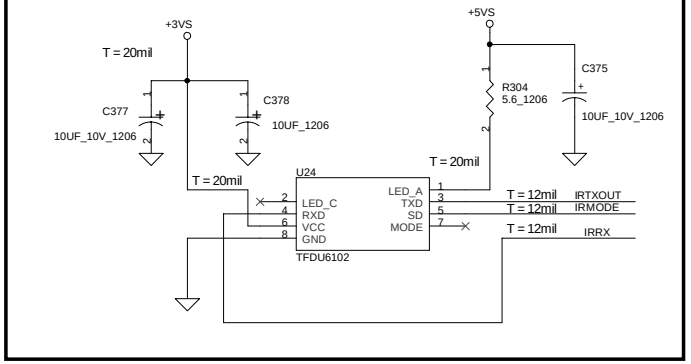


Base I/O Address
* 0 = 02Eh
1 = 04Eh

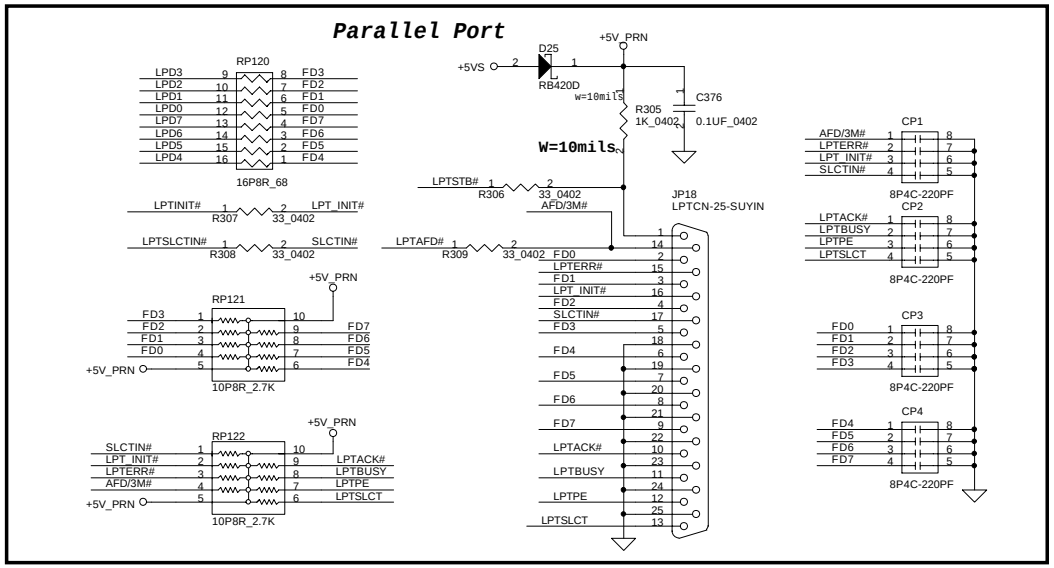
MAX3243 Transceiver



FIR Module



Parallel Port



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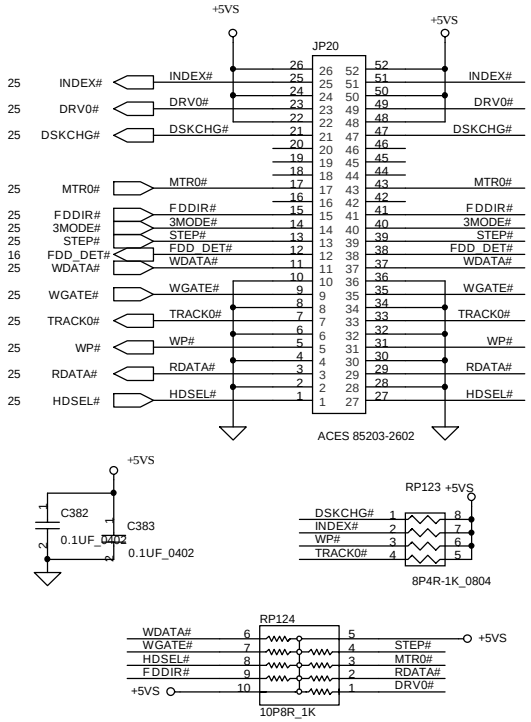
FDD CONN.



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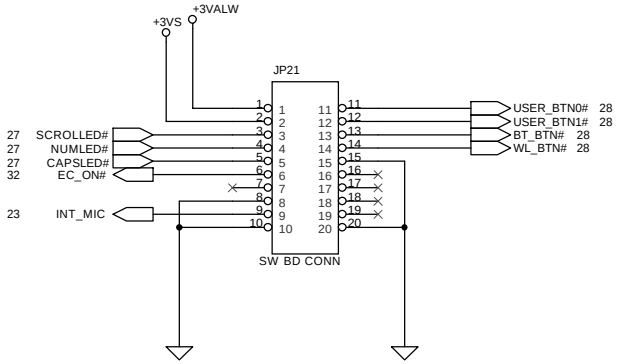

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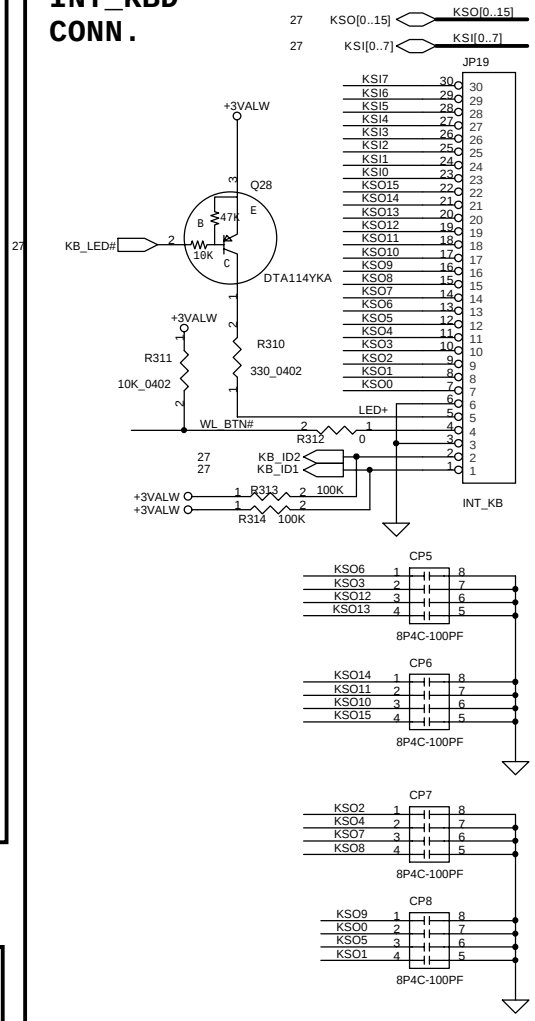
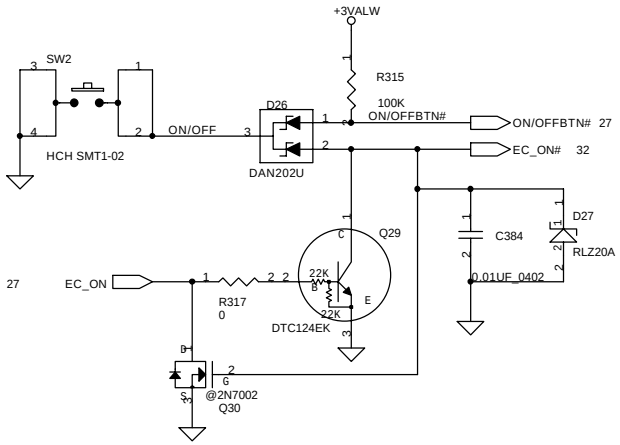
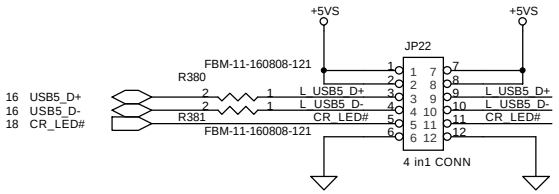


NEED CLOSEST JP18 ADD BY EMI REQUEST

ON/OFF BUTTON



5 IN 1 CONN



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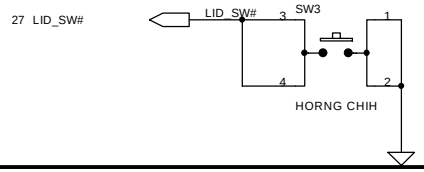

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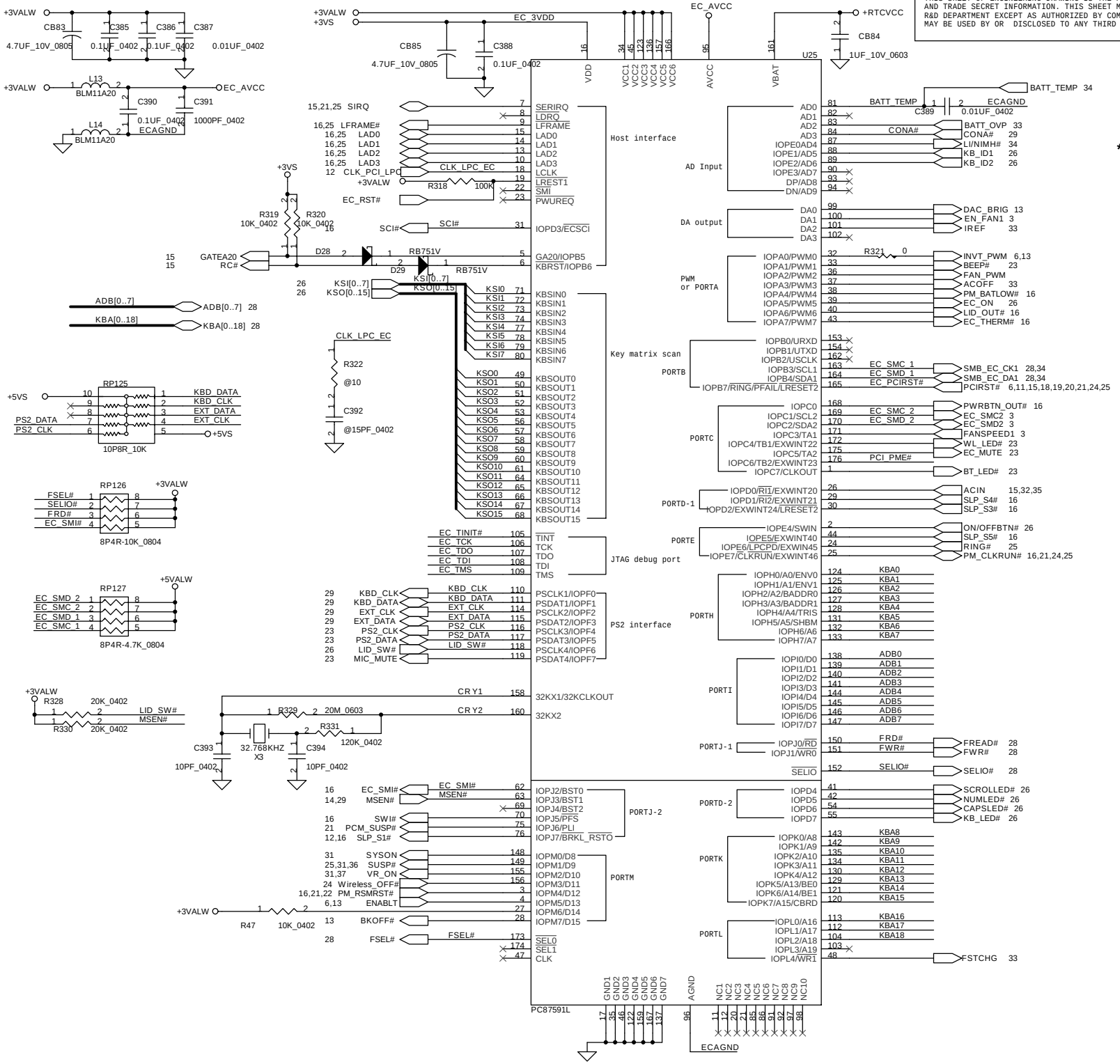
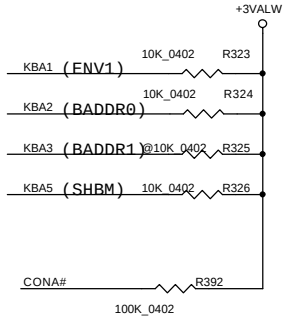
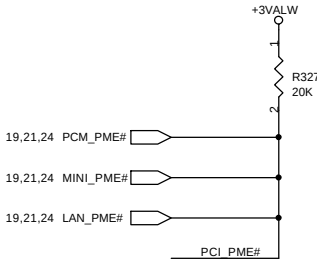


	I/O Address	
BADDR1-0	Index	Data
0 0	2E	2F
0 1	4E	4F
* 1 0	(HCFGBAH, HCFGBAL)	(HCFGBAH, HCFGBAL)+1
1 1	Reserved	

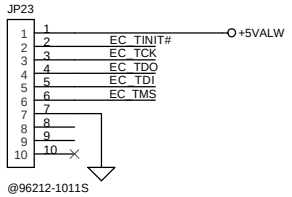
	ENV0	ENV1	TRIS
IRE	0	0	0
* OBD	0	1	0
DEV	1	0	0
PROG	1	1	0

SHBM=1: Enable shared memory with host BIOS
TRIS=1: While in IRE and OBD, float all the signals for clip-on ISE use





EC DEBUG port



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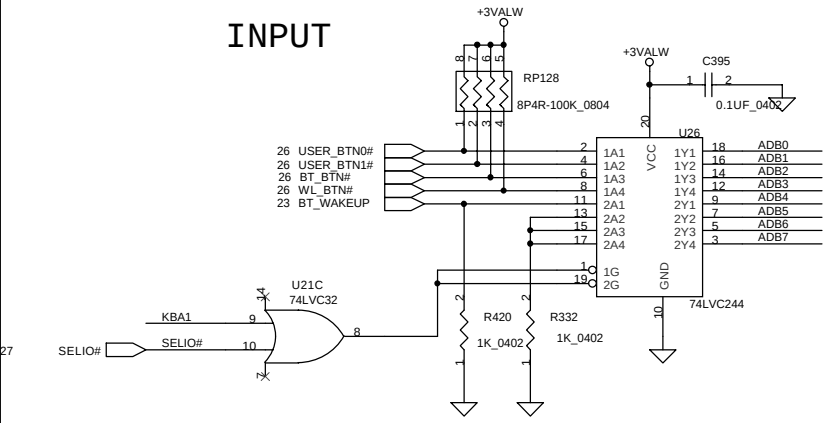
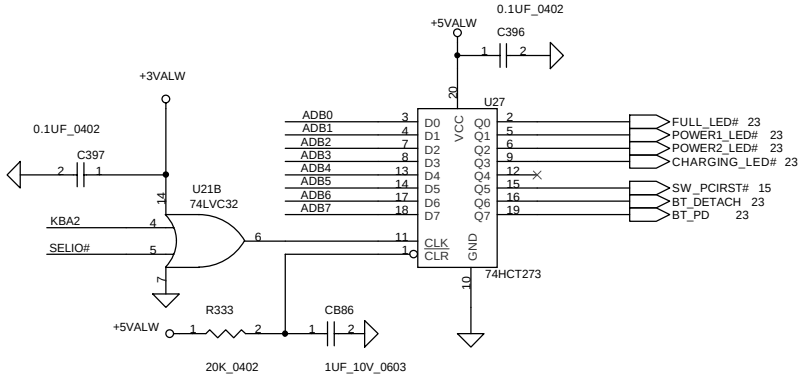
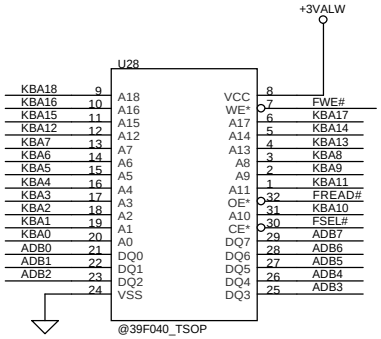
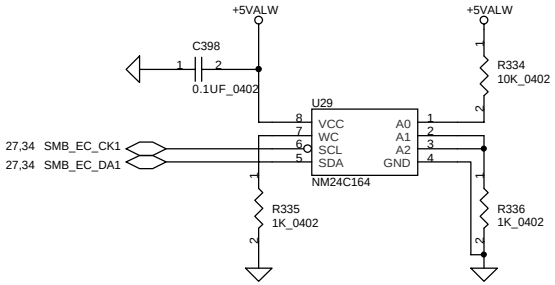
INPUT

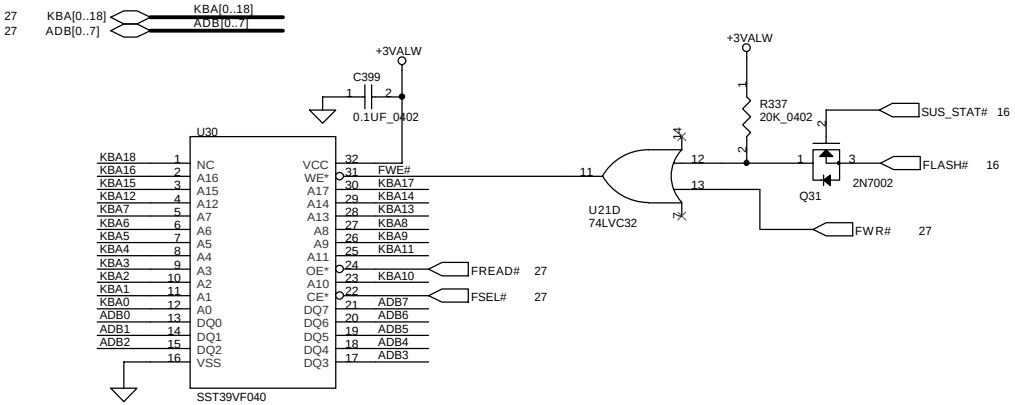


OUTPUT









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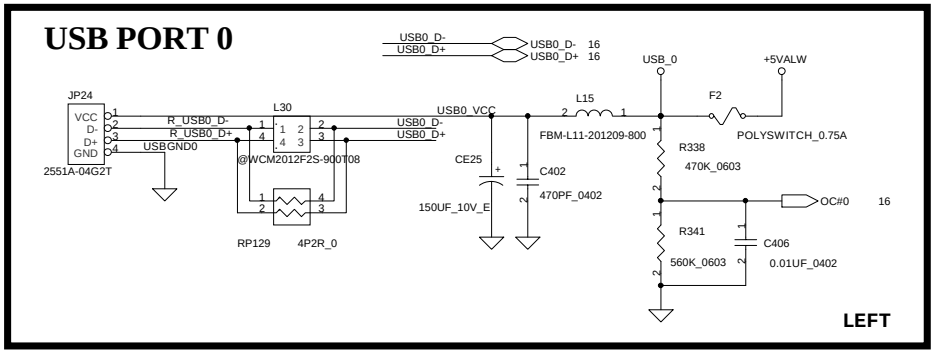
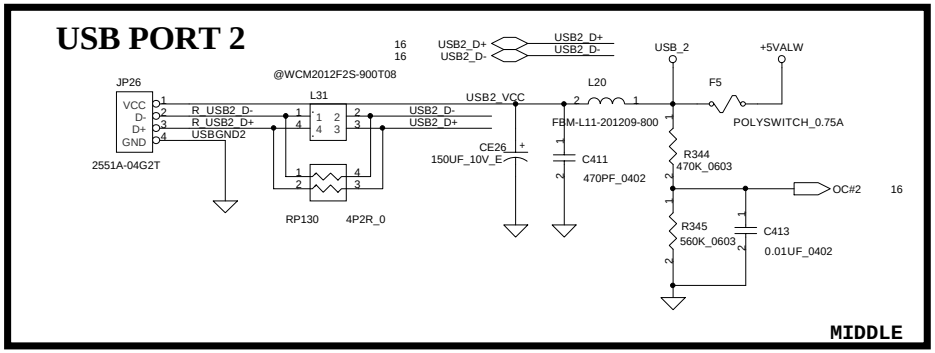
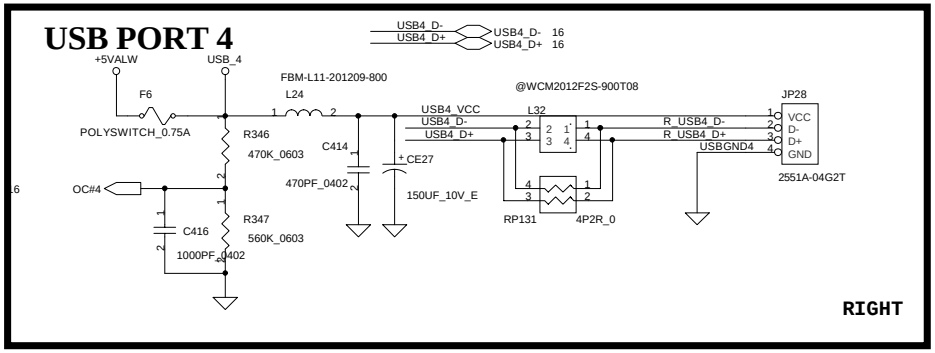
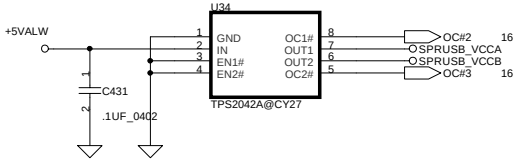
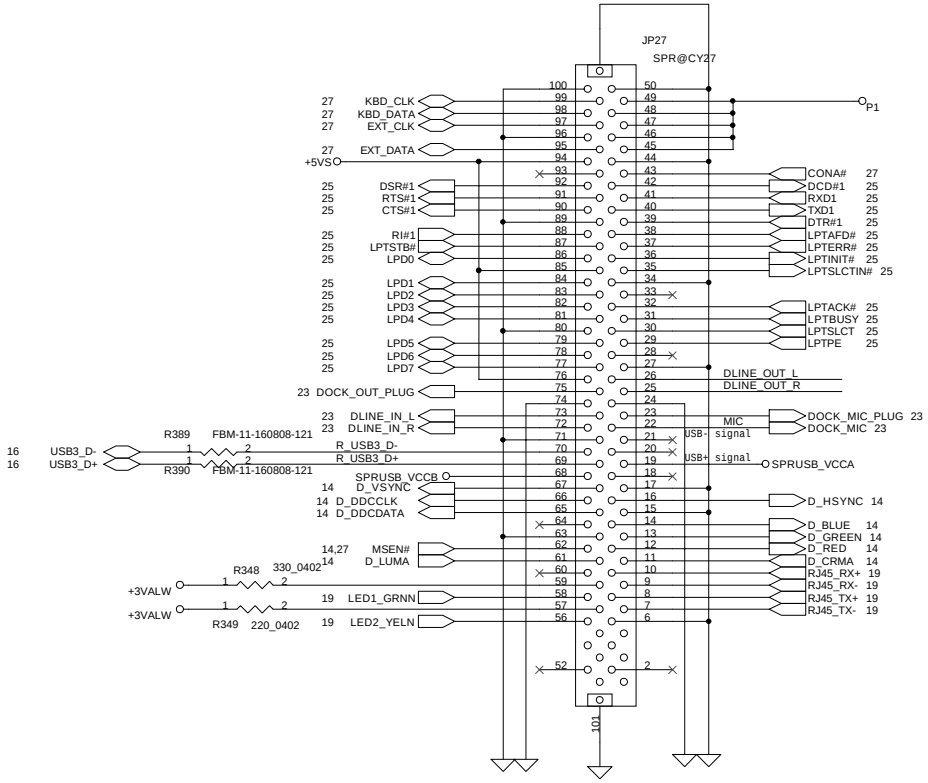


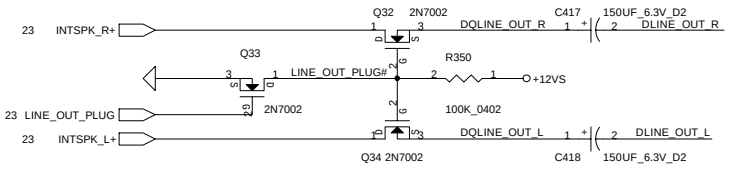






SPR CONN 204PIN





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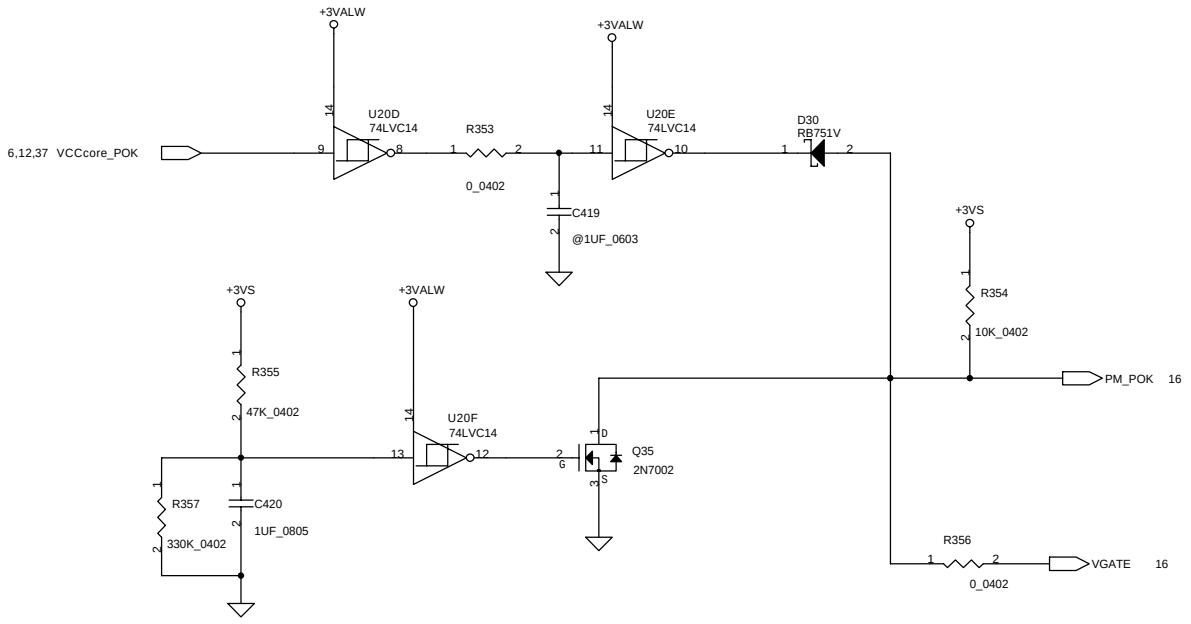

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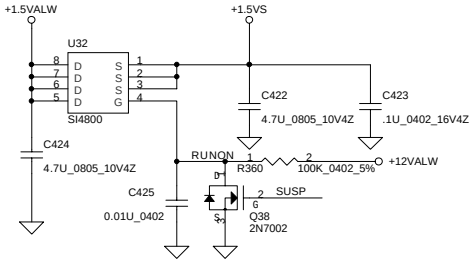
+1.5VALW To +1.5VS Transfer



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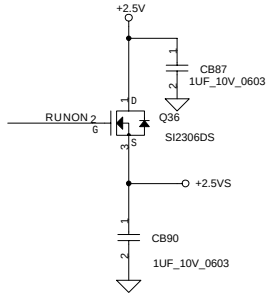

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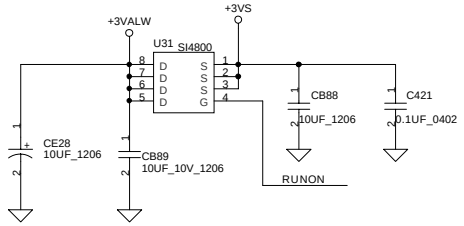

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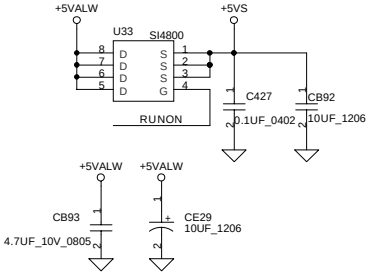
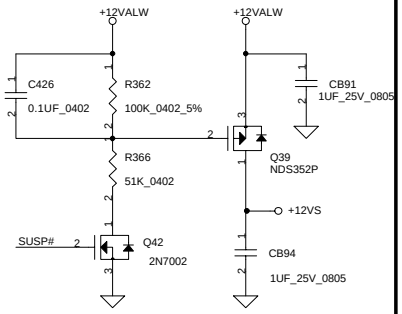
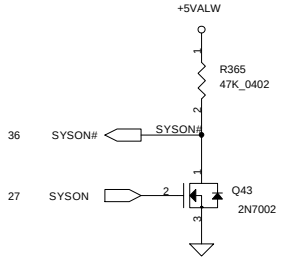
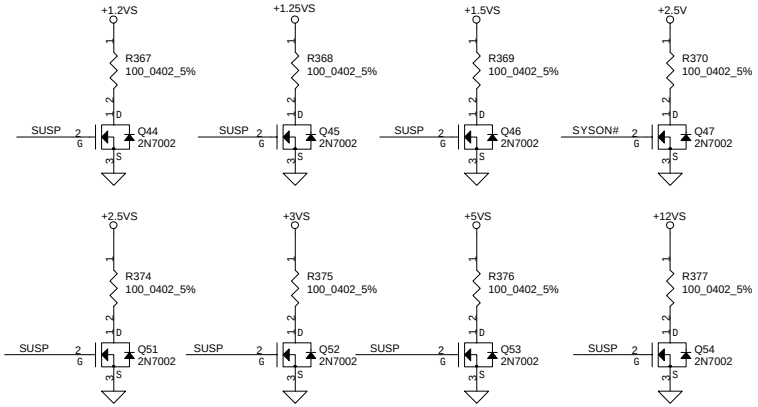


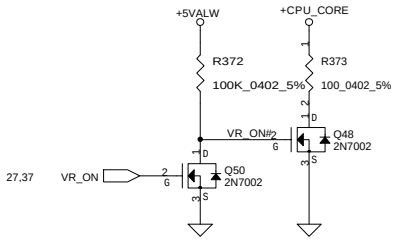
+12VALW TO +12VS Transfer

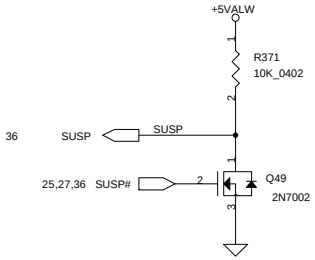




Discharge circuit







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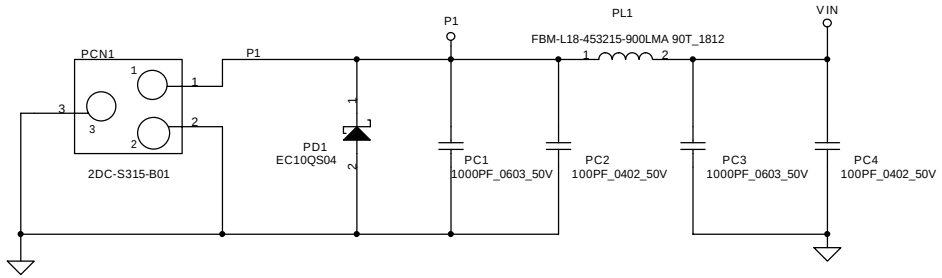
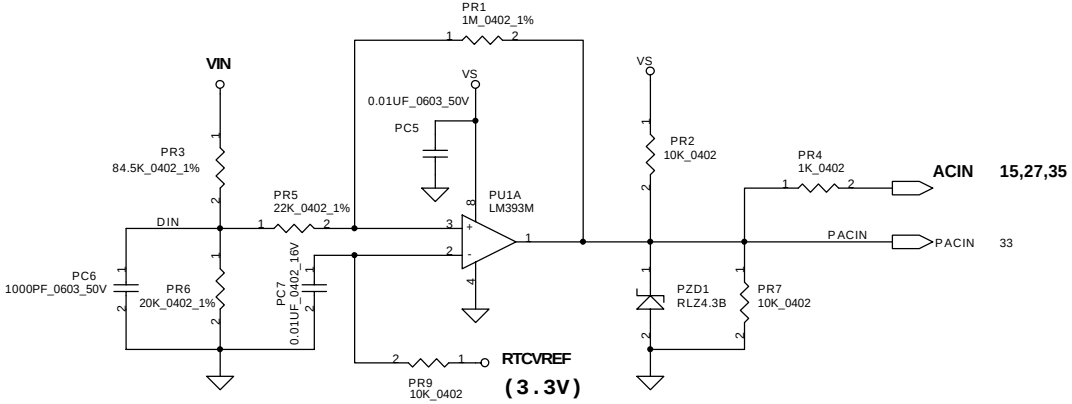
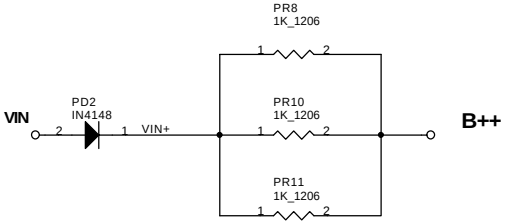
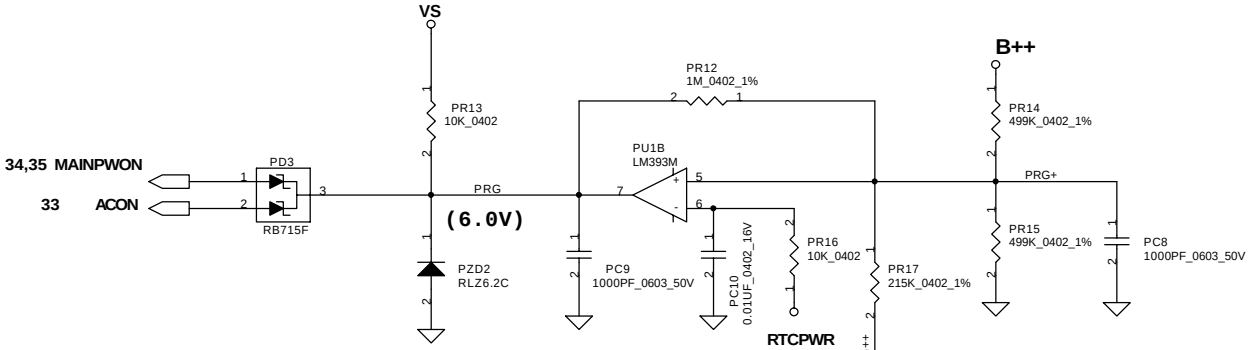


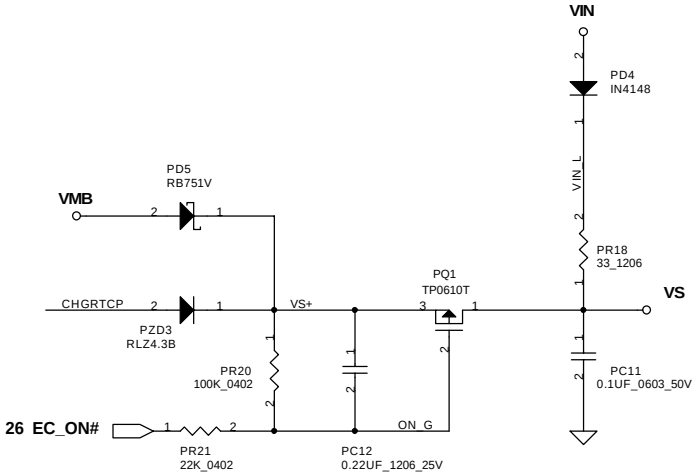
Vin Detector

High	**18.784**	**17.901**	**17.077**	**V**
Low	**17.877**	**17.043**	**16.195**	**V**







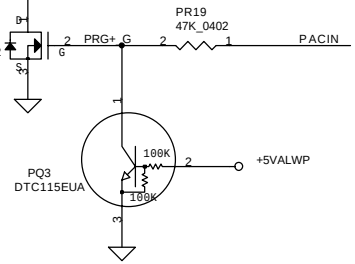


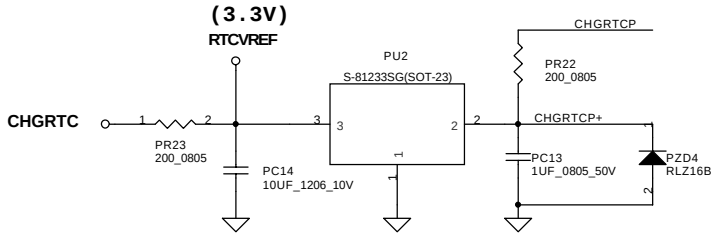
ACIN

Precharge detector		
16.6	15.9	15.2
13.48	12.93	12.09

BAT ONLY

Precharge detector		
8.597	8.247	7.904
6.310	6.101	5.683





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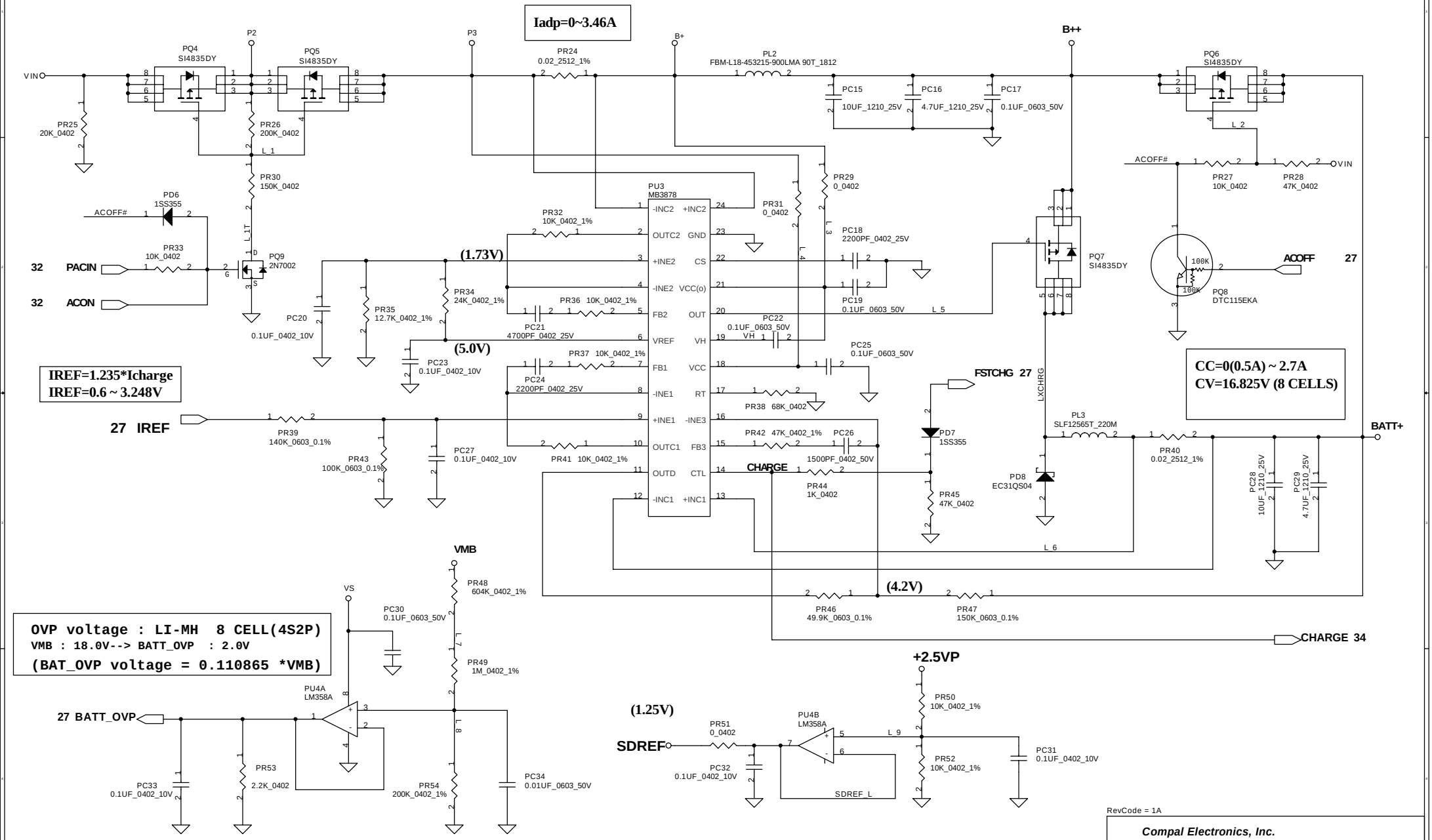

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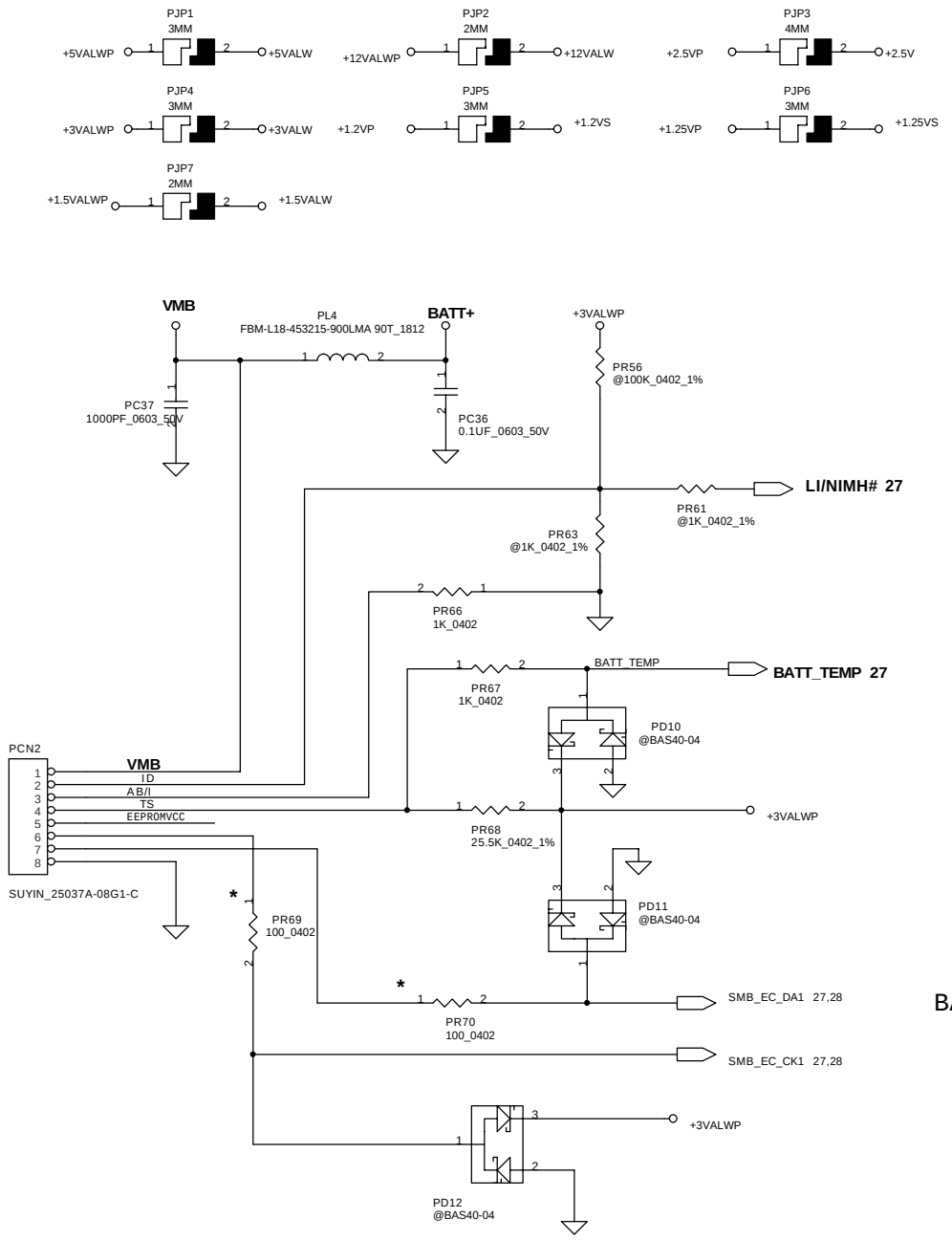
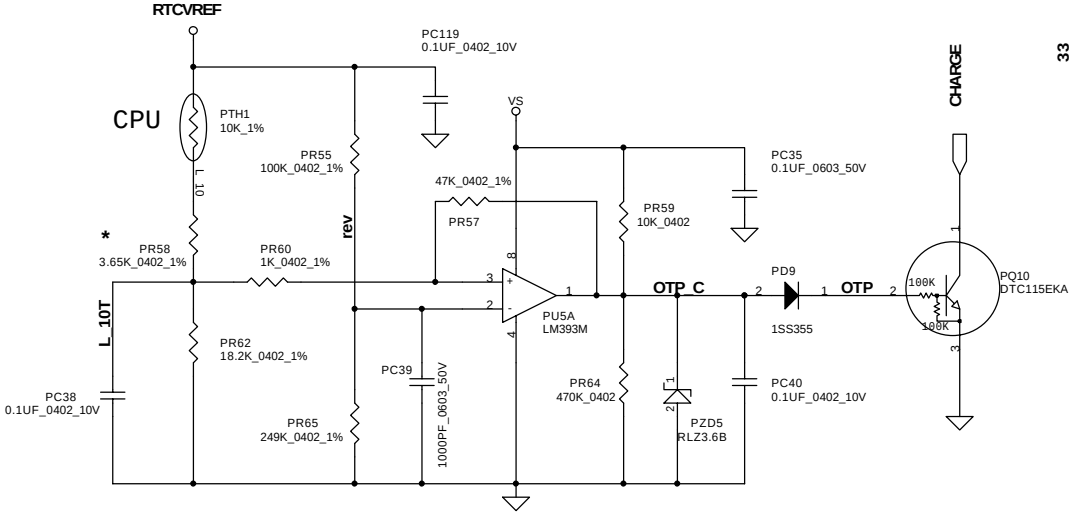
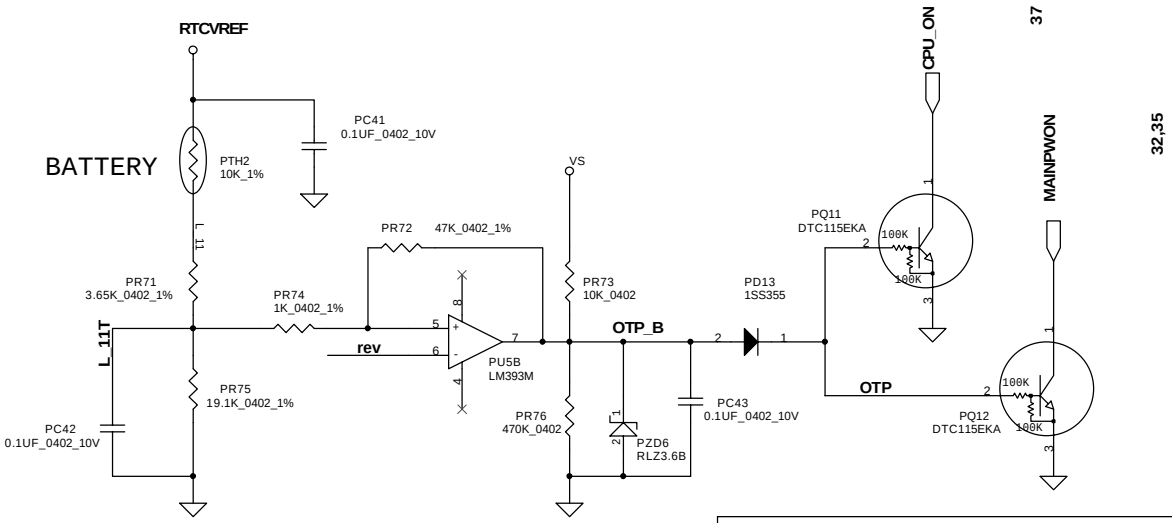


PH1 under CPU botten side :
CPU thermal protection at 90(91)+-3 degree C
Recovery at 50(51)+-3 degree C



PH2 near main Battery CONN :
BAT. thermal protection at 85(86)+-3 degree C
Recovery at 50(51) degree C



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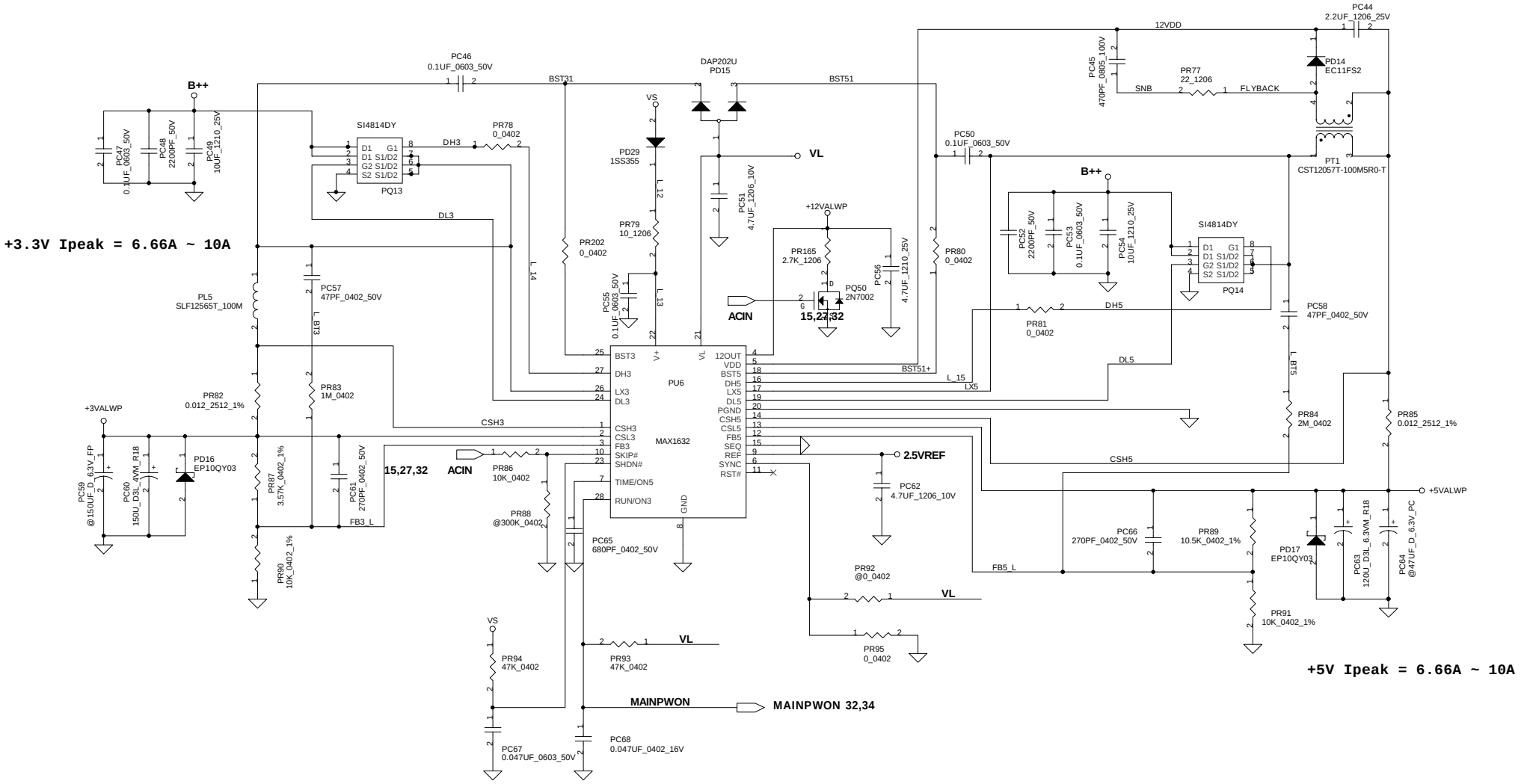

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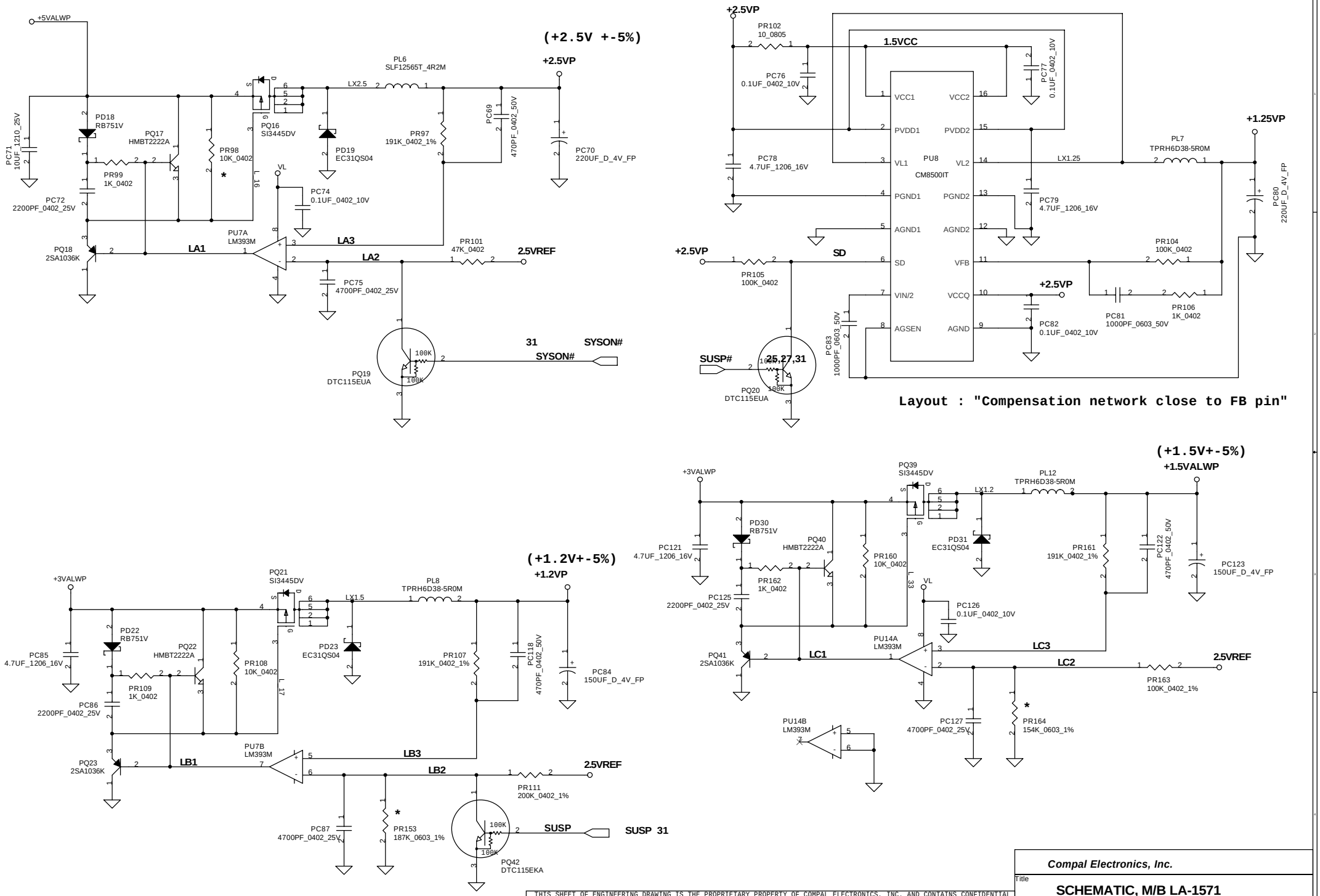

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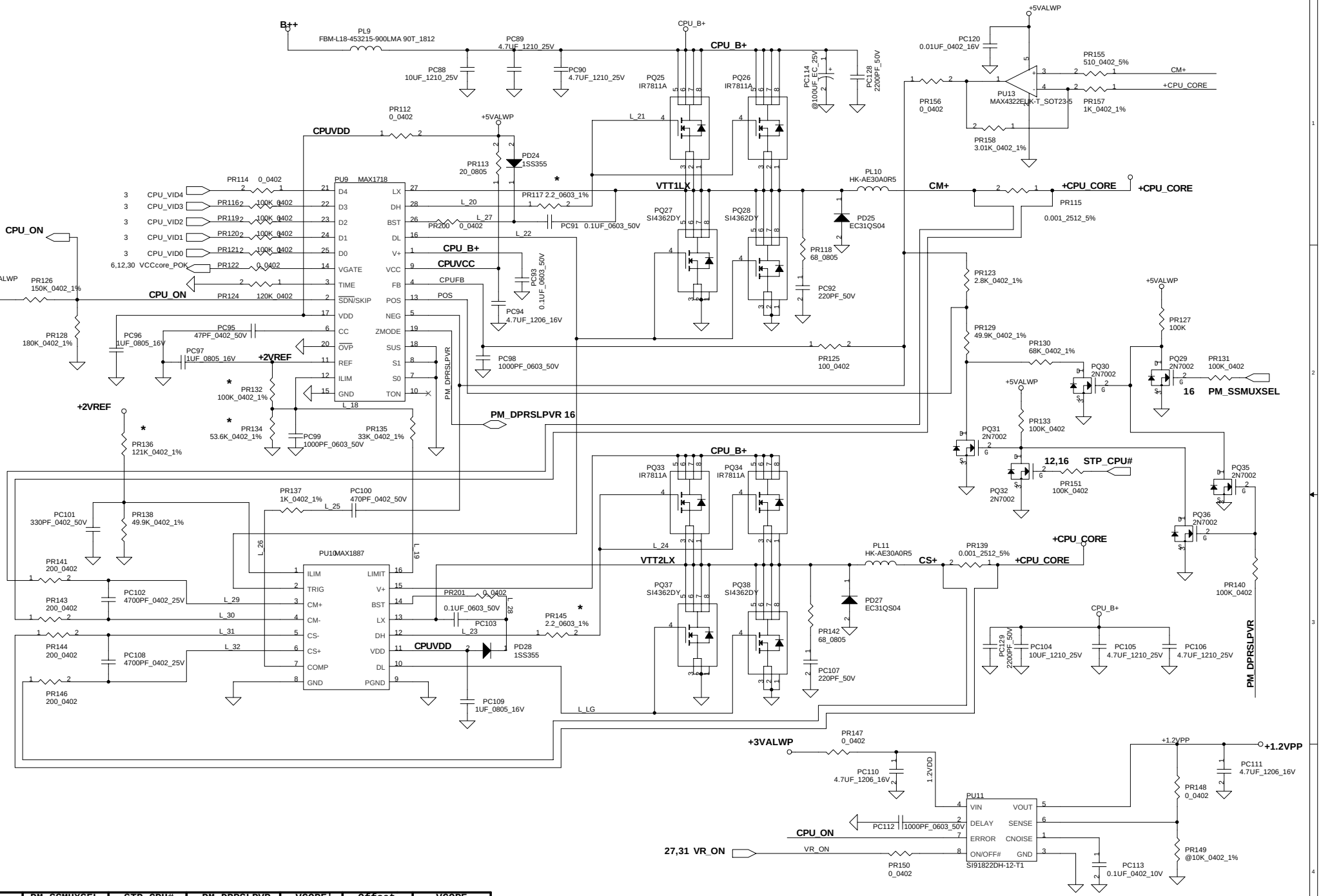

	PM_SSMUXSEL	STP_CPU#	PM_DPRSLPVR	VCORE'	Offset	VCORE
PM	1	1	0	1.30V	0%	1.30V
PM D-S	1	0	0		4.62%	1.239V
BM	0	1	0	1.20V	2.0%	1.176V
BM D-S	0	0	0		4.62%	1.144V
Deeper	X	0	1	1.0V	0%	1.0V

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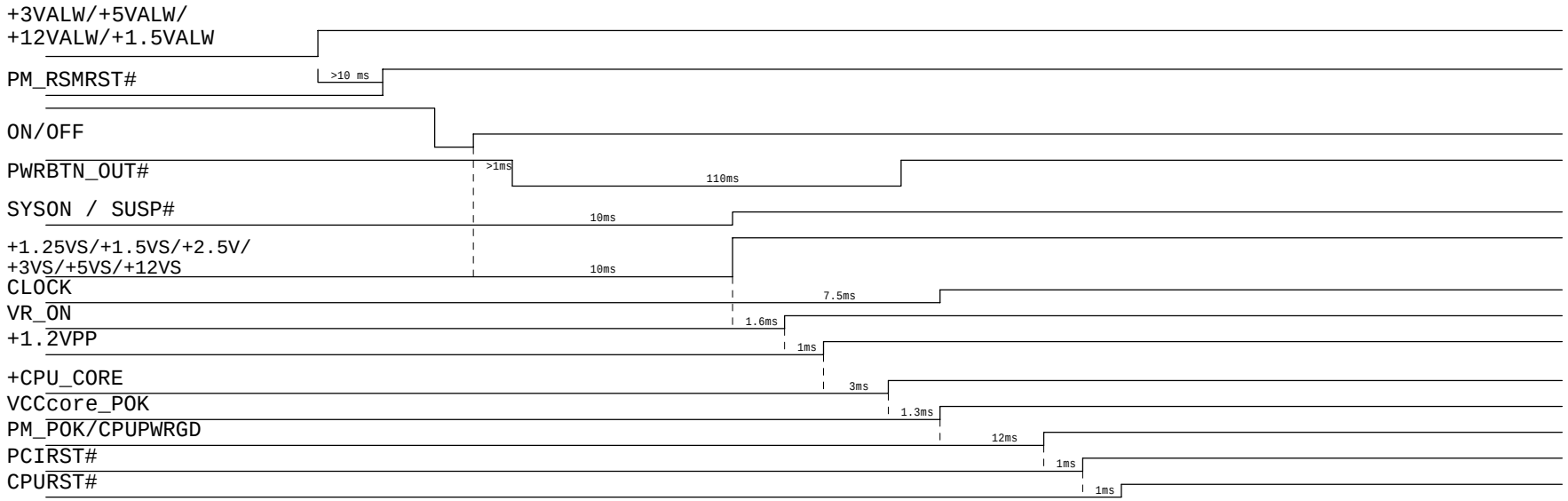

A-TEST (2002-09-09)

Fine tune power on sequence

1.C425 change to 0.01U
2.Delete R364
3.R396 change to 4.7K_0402
4.Delete R194
5.Delete R351
6.Delete R87
7.Delete R359 , Q37 , R361 , Q40 , R364 , C428 , R363 , Q41
8.Delete U10
9.Add D31

Page04 =To solve 4 sec shutdown restart issue : Delete Q3

Page03 = JP1 change to 3 pin connector(No PWM)

Page11 : EMI solution

1.Add U35 , L36 , C432 , R414 , R415 , R416

Page12 : TV-OUT issue

1. R107 , R108 changeto 4.7K

Page06 = Base on Intel spec : Delete Q6 , Q7 , R59 , R61 , C21, R87

Page20 = Delete R248 , C327

Page21 = R258 , R261 change to 47K_0402
Add R422 , R423 47K_0402
Delete R256 , C338

Page22 : Add R424 8.2K_0402

Page25 : Delete R298 , C372

Page28 : Add R420 pull low

Page29 : Add R421 , Q58

Page15 : Add R425 PULL UP

Page16 : Add R426 pull up , R427 pull down

B-TEST (2002-10-10)

Page08 : FB1,2,4,5 change to 0_0805

Page11 : R111 change to 1K_0402

Page12 : Del L36,C432,R414,R415,R416,U35,R148

Page16 : Add R428,R429 for FDD_DET#
Add R195,C235

Page23 : Del R273,R275
Add R281,C353

Page29 : Del R382,3,4,5,6,7. L30,31,32
Add RP129,130,131

Page30 : C420 change to 1UF_0805

B2-TEST (2002-12-26)

Page27 : Change RP125 to 10K

Page29 : Delete Q57, Q58 , R421 , R388 , R391

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